SECTION 3
AMPLIFIERS FOR SIGNAL CONDITIONING

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INTRODUCTION

This section examines the critical parameters of amplifiers for use in precision signal conditioning applications. Offset voltages for precision IC op amps can be as low as 10µV with corresponding temperature drifts of 0.1µV/ºC. Chopper stabilized op amps provide offsets and offset voltage drifts which cannot be distinguished from noise. Open loop gains greater than 1 million are common, along with common mode and power supply rejection ratios of the same magnitude. Applying these precision amplifiers while maintaining the amplifier performance can present significant challenges to a design engineer, i.e., external passive component selection and PC board layout.

It is important to understand that DC open-loop gain, offset voltage, power supply rejection (PSR), and common mode rejection (CMR) alone should not be the only considerations in selecting precision amplifiers. The AC performance of the amplifier is also important, even at "low" frequencies. Open-loop gain, PSR, and CMR all have relatively low corner frequencies, and therefore what may be considered "low" frequency may actually fall above these corner frequencies, increasing errors above the value predicted solely by the DC parameters. For example, an amplifier having a DC open-loop gain of 10 million and a unity-gain crossover frequency of 1MHz has a corresponding corner frequency of 0.1Hz! One must therefore consider the open loop gain at the actual *signal* frequency. The relationship between the single-pole unity-gain crossover frequency, f_u, the signal frequency, f_{sig}, and the open-loop gain $A_{VOL(fsig)}$ (measured at the signal frequency is given by:

$$A_{VOL(f_{sig})} = \frac{f_u}{f_{sig}}.$$

It the example above, the open loop gain is 10 at 100kHz, and 100,000 at 10Hz.

Loss of open loop gain at the frequency of interest can introduce distortion, especially at audio frequencies. Loss of CMR or PSR at the line frequency or harmonics thereof can also introduce errors.

The challenge of selecting the right amplifier for a particular signal conditioning application has been complicated by the sheer proliferation of various types of amplifiers in various processes (Bipolar, Complementary Bipolar, BiFET, CMOS, BiCMOS, etc.) and architectures (traditional op amps, instrumentation amplifiers, chopper amplifiers, isolation amplifiers, etc.) In addition, a wide selection of precision amplifiers are now available which operate on single supply voltages which complicates the design process even further because of the reduced signal swings and voltage input and output restrictions. Offset voltage and noise are now a more significant portion of the input signal. Selection guides and parametric search engines which can simplify this process somewhat are available on the world-wide-web (http://www.analog.com) as well as on CDROM.

In this section, we will first look at some key performance specifications for precision op amps. Other amplifiers will then be examined such as instrumentation amplifiers, chopper amplifiers, and isolation amplifiers. The implications of single supply operation will be discussed in detail because of their significance in today's designs, which often operate from batteries or other low power sources.

AMPLIFIERS FOR SIGNAL CONDITIONING

■ Input Offset Voltage	<100µV
■ Input Offset Voltage Drift	<1µV/°C
■ Input Bias Current	<2nA
■ Input Offset Current	<2nA
■ DC Open Loop Gain	>1,000,000
■ Unity Gain Bandwidth Product, f_u	500kHz - 5MHz
■ Always Check Open Loop Gain at Signal Frequency!	
■ 1/f (0.1Hz to 10Hz) Noise	<1µV p-p
■ Wideband Noise	<10nV/√Hz
■ CMR, PSR	>100dB

- Single Supply Operation
- Power Dissipation

Figure 3.1

PRECISION OP AMP CHARACTERISTICS

Input Offset Voltage

Input offset voltage error is usually one of the largest error sources for precision amplifier circuit designs. However, it is a systemic error and can usually be dealt with by using a manual offset null trim or by system calibration techniques using a microcontroller or microprocessor. Both solutions carry a cost penalty, and today's precision op amps offer initial offset voltages as low as 10µV for bipolar devices, and far less for chopper stabilized amplifiers. With low offset amplifiers, it is possible to eliminate the need for manual trims or system calibration routines.

Measuring input offset voltages of a few microvolts requires that the test circuit does not introduce more error than the offset voltage itself. Figure 3.2 shows a circuit for measuring offset voltage. The circuit amplifies the input offset voltage by the noise gain (1001). The measurement is made at the amplifier output using an accurate digital voltmeter. The offset referred to the input (RTI) is calculated by dividing the output voltage by the noise gain. The small source resistance seen at R1||R2 results in negligible bias current contribution to the measured offset voltage. For example, 2nA bias current flowing through the 10Ω resistor produces a 0.02μV error referred to the input.

MEASURING INPUT OFFSET VOLTAGE

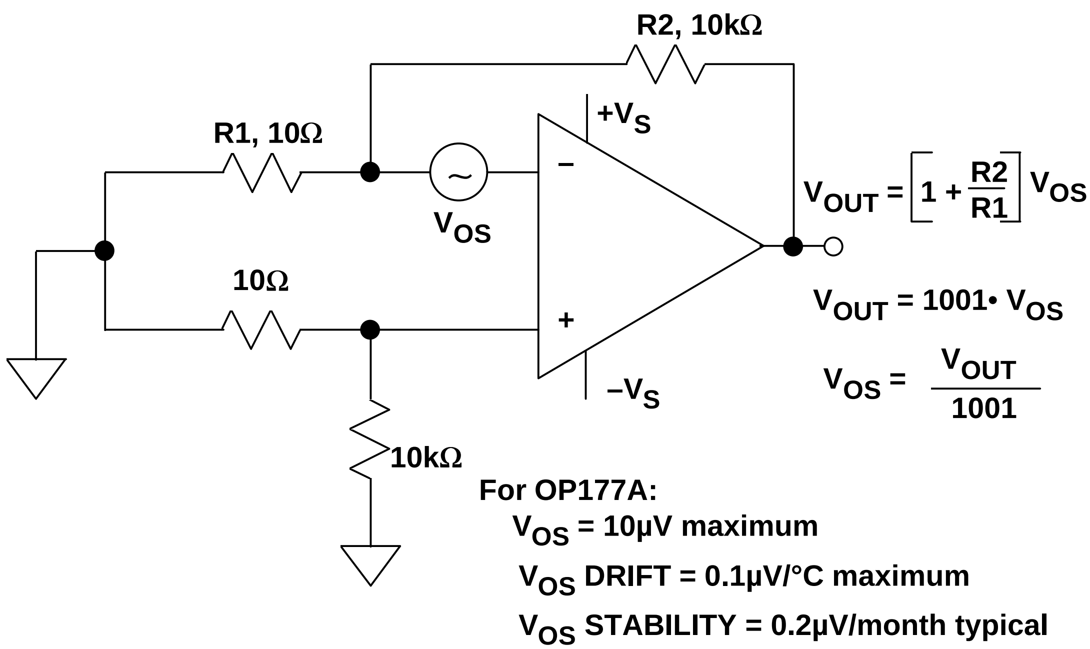


Figure 3.2

As simple as it looks, this circuit may give inaccurate results. The largest potential source of error comes from parasitic thermocouple junctions formed where two different metals are joined. The thermocouple voltage formed by temperature difference between two junctions can range from 2μV/ºC to more than 40μV/ºC. Note that in the circuit additional resistors have been added to the non-inverting input in order to exactly match the thermocouple junctions in the inverting input path.

The accuracy of the measurement depends on the mechanical layout of the components and how they are placed on the PC board. Keep in mind that the two connections of a component such as a resistor create two equal, but opposite polarity thermoelectric voltages (assuming they are connected to the same metal, such as the copper trace on a PC board) which cancel each other *assuming both are at exactly the*

same temperature. Clean connections and short lead lengths help to minimize temperature gradients and increase the accuracy of the measurement.

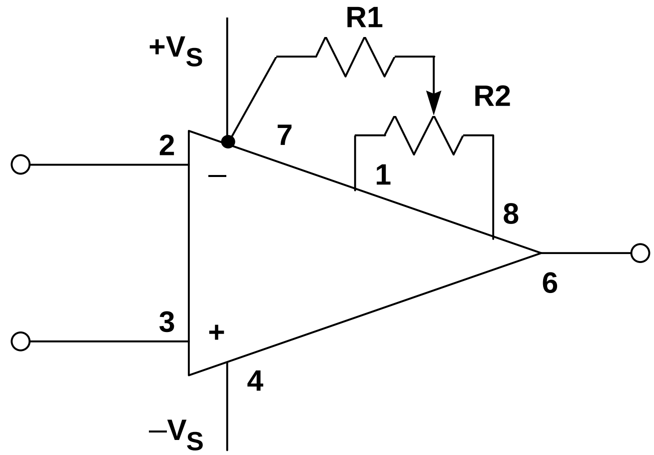
Airflow should be minimal so that all the thermocouple junctions stabilize at the same temperature. In some cases, the circuit should be placed in a small closed container to eliminate the effects of external air currents. The circuit should be placed flat on a surface so that convection currents flow up and off the top of the board, not across the components as would be the case if the board was mounted vertically.

Measuring the offset voltage shift over temperature is an even more demanding challenge. Placing the printed circuit board containing the amplifier being tested in a small box or plastic bag with foam insulation prevents the temperature chamber air current from causing thermal gradients across the parasitic thermocouples. If cold testing is required, a dry nitrogen purge is recommended. Localized temperature cycling of the amplifier itself using a Thermostream-type heater/cooler may be an alternative, however these units tend to generate quite a bit of airflow which can be troublesome.

In addition to temperature related drift, the offset voltage of an amplifier changes as time passes. This aging effect is generally specified as *long-term stability* in µV/month, or µV/1000 hours, but this is misleading. Since aging is a "drunkard's walk" phenomenon, it is proportional to the *square root* of the elapsed time. An aging rate of 1µV/1000 hours becomes about 3µV/year, not 9µV/year. Long-term stability of the OP177 and the AD707 is approximately 0.3µV/month. This refers to a time period *after* the first 30 days of operation. Excluding the initial hour of operation, changes in the offset voltage of these devices during the first 30 days of operation are typically less than 2µV.

As a general rule of thumb, it is prudent to control amplifier offset voltage by device selection whenever possible, bus sometimes trim may be desired. Many precision op amps have pins available for optional offset null. Generally, two pins are joined by a potentiometer, and the wiper goes to one of the supplies through a resistor as shown in Figure 3.3. If the wiper is connected to the wrong supply, the op amp will probably be destroyed, so the data sheet instructions must be carefully observed! The range of offset adjustment in a precision op amp should be no more than two or three times the maximum offset voltage of the lowest grade device, in order to minimize the sensitivity of these pins. The voltage gain of an op amp between its offset adjustment pins and its output may actually be greater than the gain at its signal inputs! It is therefore very important to keep these pins free of noise. It is inadvisable to have long leads from an op amp to a remote potentiometer. To minimize any offset error due to supply current, connect R1 directly to the pertinent device supply pin, such as pin 7 shown in the diagram.

OP177/AD707 OFFSET ADJUSTMENT PINS



- **R1 = 10kΩ, R2 = 2kΩ , OFFSET ADJUST RANGE = 200µV**
- **R1 = 0, R1 = 20kΩ , OFFSET ADJUST RANGE = 3mV**

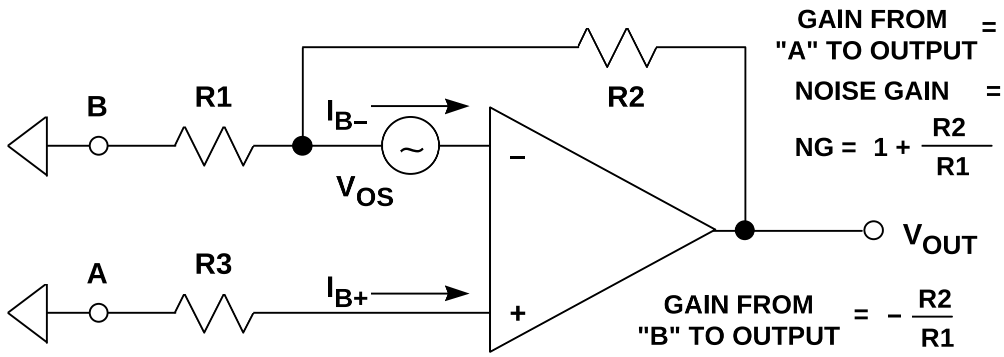
Figure 3.3

It is important to note that the offset drift of an op amp with temperature will vary with the setting of its offset adjustment. In most cases a bipolar op amp will have minimum drift at minimum offset. The offset adjustment pins should therefore be used only to adjust the op amp's own offset, not to correct any system offset errors, since this would be at the expense of increased temperature drift. The drift penalty for a JFET input op amp is much worse than for a bipolar input and is in the order of 4µV/ºC for each millivolt of nulled offset voltage. It is generally better to control the offset voltage by proper selection of devices and device grades. Dual, triple, quad, and single op amps in small packages do not generally have null capability because of pin count limitations, and offset adjustments must be done elsewhere in the system when using these devices. This can be accomplished with minimal impact on drift by a universal trim, which sums a small voltage into the input.

Input Offset Voltage and Input Bias Current Models

Thus far, we have considered only the op amp input offset voltage. However, the input bias currents also contribute to offset error as shown in the generalized model of Figure 3.4. It is useful to refer all offsets to the op amp input (RTI) so that they can be easily compared with the input signal. The equations in the diagram are given for the total offset voltage referred to input (RTI) and referred to output (RTO).

OP AMP TOTAL OFFSET VOLTAGE MODEL



- $\text{OFFSET (RTO)} = V_{OS}\left[1+\frac{R2}{R1}\right] + I_{B+} \cdot R3\left[1+\frac{R2}{R1}\right] - I_{B-} \cdot R2$
- $\text{OFFSET (RTI)} = V_{OS} + I_{B+} \cdot R3 - I_{B-}\left[\frac{R1 \cdot R2}{R1+R2}\right]$

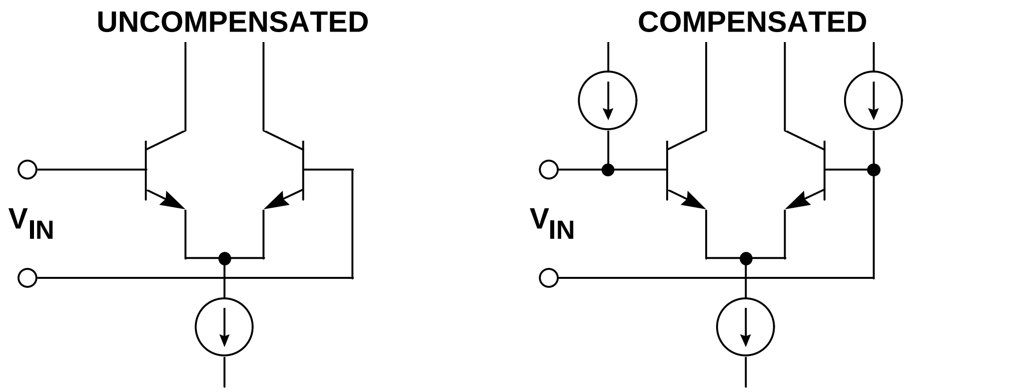
FOR BIAS CURRENT CANCELLATION:

$\text{OFFSET (RTI)} = V_{OS} \quad \text{IF } I_{B+} = I_{B-} \text{ AND } R3 = \frac{R1 \cdot R2}{R1+R2}$

Figure 3.4

For a precision op amp having a standard bipolar input stage using either PNPs or NPNs, the input bias currents are typically 50nA to 400nA and are well matched. By making R3 equal to the parallel combination of R1 and R2, their effect on the net RTI and RTO offset voltage is approximately canceled, thus leaving the offset current, i.e., the difference between the input currents as an error. This current is usually an order of magnitude lower than the bias current specification. This scheme, however, does not work for bias-current compensated bipolar op amps (such as the OP177 and the AD707) as shown in Figure 3.5. Bias-current compensated input stages have most of the good features of the simple bipolar input stage: low offset and drift, and low voltage noise. Their bias current is low and fairly stable over temperature. The additional current sources reduce the net bias currents typically to between 0.5nA and 10nA. However, the signs of the + and – input bias currents may or may not be the same, and they are not well matched, but are very low. Typically, the specification for the *offset current* (the difference between the + and – input bias currents) in bias-current compensated op amps is generally about the same as the individual bias currents. In the case of the standard bipolar differential pair with no bias-current compensation, the offset current specification is typically five to ten times lower than the bias current specification.

INPUT BIAS CURRENT COMPENSATED OP AMPS



- MATCHED BIAS CURRENTS
- SAME SIGN
- 50nA - 10µA
- 50pA - 5nA (Super Beta)
- $I_{OFFSET} << I_{BIAS}$

- LOW, UNMATCHED BIAS CURRENTS
- CAN HAVE DIFFERENT SIGNS
- 0.5nA - 10nA
- HIGHER CURRENT NOISE
- $I_{OFFSET} \approx I_{BIAS}$

Figure 3.5

DC Open Loop Gain Nonlinearity

It is well understood that in order to maintain accuracy, a precision amplifier's DC open loop gain, A_{VOL}, should be high. This can be seen by examining the equation for the closed loop gain:

$$\text{Closed Loop Gain} = A_{VCL} = \frac{NG}{1 + \frac{NG}{A_{VOL}}}.$$

Noise gain (NG) is simply the gain seen by a small voltage source in series with the op amp input and is also the amplifier signal gain in the noninverting mode. If A_{VOL} in the above equation is infinite, the closed loop gain is exactly equal to the noise gain. However, for finite values of A_{VOL}, there is a closed loop gain error given by the equation:

$$\%\text{Gain Error} = \frac{NG}{NG + A_{VOL}} \times 100\% \approx \frac{NG}{A_{VOL}} \times 100\%, \text{ for } NG << A_{VOL}.$$

Notice from the equation that the percent gain error is directly proportional to the noise gain, therefore the effects of finite A_{VOL} are less for low gain. The first example in Figure 3.6 where the noise gain is 1000 shows that for an open loop gain of 2 million, there is a gain error of about 0.05%. If the open loop gain stays constant over temperature and for various output loads and voltages, the gain error can be calibrated out of the measurement, and there is then no overall system gain error. If, however, the open loop gain *changes*, the closed loop gain will also change, thereby introducing a *gain uncertainty*. In the second example in the figure, an A_{VOL} decrease to 300,000 produces a gain error of 0.33%, introducing a *gain*

uncertainty of 0.28% in the closed loop gain. In most applications, using the proper amplifier, the resistors around the circuit will be the largest source of gain error.

CHANGES IN DC OPEN LOOP GAIN CAUSE CLOSED LOOP GAIN UNCERTAINTY

- **"IDEAL" CLOSED LOOP GAIN = NOISE GAIN = NG**
- **ACTUAL CLOSED LOOP GAIN =** $\dfrac{NG}{1+\dfrac{NG}{A_{VOL}}}$
- **% CLOSED LOOP GAIN ERROR =** $\dfrac{NG}{NG + A_{VOL}} \times 100\% \approx \dfrac{NG}{A_{VOL}} \times 100\%$

  - **Assume A_{VOL} = 2,000,000, NG = 1,000**
    %GAIN ERROR ≈ 0.05%
  - **Assume A_{VOL} Drops to 300,000**
    %GAIN ERROR ≈ 0.33%
  - **CLOSED LOOP GAIN UNCERTAINTY**
    = 0.33% – 0.05% = 0.28%

Figure 3.6

Changes in the output voltage level and the output loading are the most common causes of changes in the open loop gain of op amps. A change in open loop gain with signal level produces *nonlinearity* in the closed loop gain transfer function which cannot be removed during system calibration. Most op amps have fixed loads, so A_{VOL} changes with load are not generally important. However, the sensitivity of A_{VOL} to output signal level may increase for higher load currents.

The severity of the nonlinearity varies widely from device type to device type, and is generally not specified on the data sheet. The minimum A_{VOL} is always specified, and choosing an op amp with a high A_{VOL} will minimize the probability of gain nonlinearity errors. Gain nonlinearity can come from many sources, depending on the design of the op amp. One common source is thermal feedback. If temperature shift is the sole cause of the nonlinearity error, it can be assumed that minimizing the output loading will help. To verify this, the nonlinearity is measured with no load and then compared to the loaded condition.

An oscilloscope X-Y display test circuit for measuring DC open loop gain nonlinearity is shown in Figure 3.7. The same precautions previously discussed relating to the offset voltage test circuit must be observed in this circuit. The amplifier is configured for a signal gain of –1. The open loop gain is defined as the change in output voltage divided by the change in the input offset voltage. However, for large values of A_{VOL}, the offset may change only a few microvolts over the entire output voltage swing. Therefore the divider consisting of the 10Ω resistor and R_G (1M Ω) forces the voltage V_Y to be :

$$V_Y = \left[1 + \frac{R_G}{10\Omega}\right] V_{OS} = 100{,}001 \bullet V_{OS}.$$

The value of R_G is chosen to give measurable voltages at V_Y depending on the expected values of V_{OS}.

CIRCUIT MEASURES OPEN LOOP GAIN NONLINEARITY

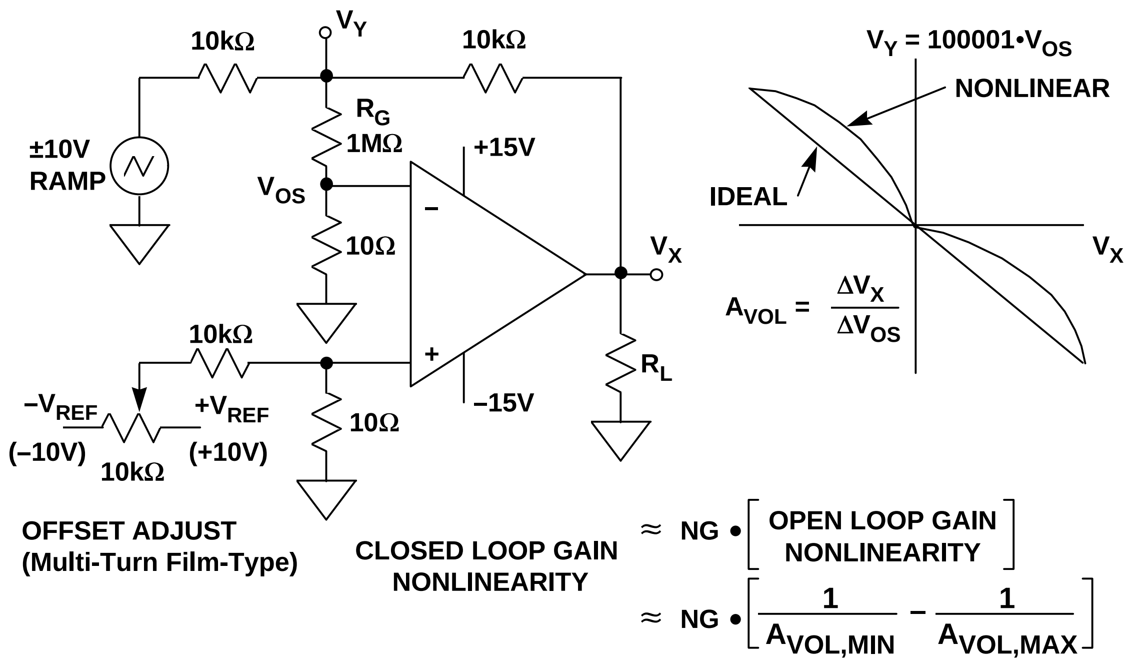


Figure 3.7

The ±10V ramp generator output is multiplied by the signal gain, –1, and forces the op amp output voltage V_X to swing from +10V to –10V. Because of the gain factor applied to the offset voltage, the offset adjust potentiometer is added to allow the initial output offset to be set to zero. The resistor values chosen will null an input offset voltage of up to ±10mV. Stable 10V voltage references (AD688) should be used at each end of the potentiometer to prevent output drift. *Also, the frequency of the ramp generator must be quite low, probably no more than a fraction of 1Hz because of the low corner frequency of the open loop gain (0.1Hz for the OP177).*

The plot on the right-hand side of Figure 3.7 shows V_Y plotted against V_X. If there is no gain nonlinearity the graph will have a constant slope, and A_{VOL} is calculated as follows:

$$A_{VOL} = \frac{\Delta V_X}{\Delta V_{OS}} = \left[1 + \frac{R_G}{10\Omega}\right]\left[\frac{\Delta V_X}{\Delta V_Y}\right] = 100{,}001 \bullet \left[\frac{\Delta V_X}{\Delta V_Y}\right].$$

If there is nonlinearity, A_{VOL} will vary as the output signal changes. The approximate open loop gain nonlinearity is calculated based on the maximum and minimum values of A_{VOL} over the output voltage range:

$$\text{Open Loop Gain Nonlinearity} = \frac{1}{A_{VOL,MIN}} - \frac{1}{A_{VOL,MAX}}.$$

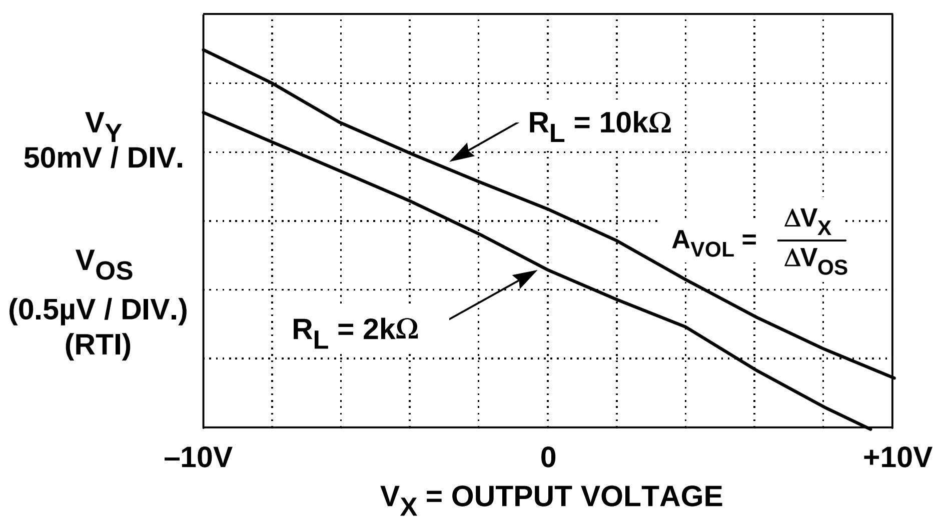
The closed loop gain nonlinearity is obtained by multiplying the open loop gain nonlinearity by the noise gain, NG:

$$\text{Closed Loop Gain Nonlinearity} \approx NG \bullet \left[\frac{1}{A_{VOL,MIN}} - \frac{1}{A_{VOL,MAX}}\right].$$

In the ideal case, the plot of V_{OS} versus V_X would have a constant slope, and the reciprocal of the slope is the open loop gain, A_{VOL}. A horizontal line with zero slope would indicate infinite open loop gain. In an actual op amp, the slope may change across the output range because of nonlinearity, thermal feedback, etc. In fact, the slope can even change sign.

Figure 3.8 shows the V_Y (and V_{OS}) versus V_X plot for the OP177 precision op amp. The plot is shown for two different loads, 2kΩ and 10kΩ. The reciprocal of the slope is calculated based on the end points, and the average A_{VOL} is about 8 million. The maximum and minimum values of A_{VOL} across the output voltage range are measured to be approximately 9.1 million, and 5.7 million, respectively. This corresponds to an open loop gain nonlinearity of about 0.07ppm. Thus, for a noise gain of 100, the corresponding closed loop gain nonlinearity is about 7ppm.

OP177 GAIN NONLINEARITY



A_{VOL} (AVERAGE) ≈ 8 million

$A_{VOL,MAX}$ ≈ 9.1 million, $A_{VOL,MIN}$ ≈ 5.7million

OPEN LOOP GAIN NONLINEARITY ≈ 0.07ppm

CLOSED LOOP GAIN NONLINEARITY ≈ NG×0.07ppm

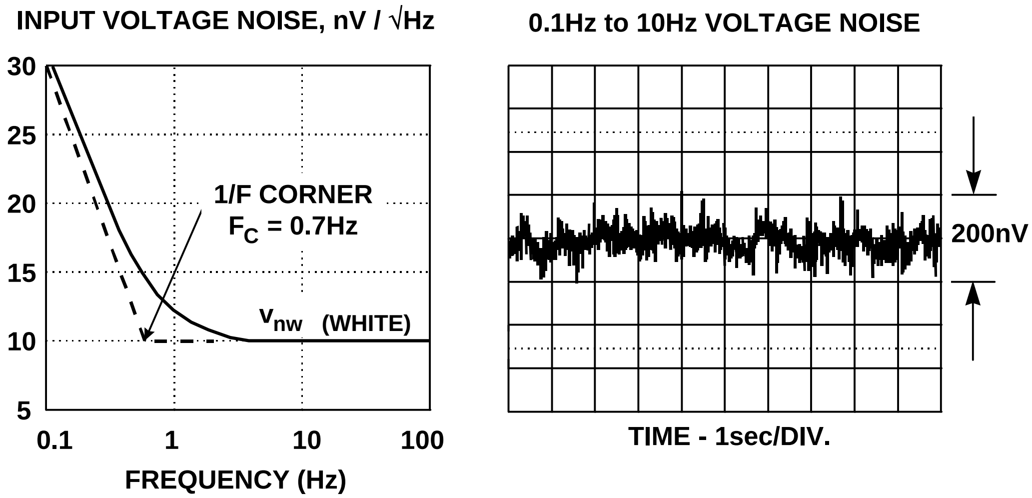
Figure 3.8

Op Amp Noise

The three noise sources in an op amp circuit are the voltage noise of the op amp, the current noise of the op amp (there are two uncorrelated sources, one in each input),

and the Johnson noise of the resistances in the circuit. Op amp noise has two components - "white" noise at medium frequencies and low frequency "1/f" noise, whose spectral density is inversely proportional to the square root of the frequency. It should be noted that, though both the voltage and the current noise may have the same characteristic behavior, in a particular amplifier the 1/f corner frequency is not necessarily the same for voltage and current noise (it is usually specified for the voltage noise as shown in Figure 3.9.

INPUT VOLTAGE NOISE FOR OP177/AD707



- $V_{n,rms}(F_H, F_L) = v_{nw}\sqrt{F_C \ln\left[\frac{F_H}{F_L}\right] + (F_H - F_L)}$
- For F_L = 0.1Hz, F_H = 10Hz, v_{nw} = 10nV/√Hz, F_C = 0.7Hz:
  - $V_{n,rms}$ = 36nV
  - $V_{n,pp}$ = 6.6 × 36nV = 238nV

Figure 3.9

The low frequency noise is generally known as 1/f noise (the noise power obeys a 1/f law - the noise voltage or noise current is proportional to 1/√f). The frequency at which the 1/f noise spectral density equals the white noise is known as the *1/f corner frequency*, F_C, and is a figure of merit for an op amp, with low corner frequencies indicating better performance. Values of 1/f corner frequency vary from less than 1Hz high accuracy bipolar op amps like the OP177/AD707, several hundred Hz for the AD743/745 FET-input op amps, to several thousands of Hz for some high speed op amps where process compromises favor high speed rather than low frequency noise.

For the OP177/AD707 shown in Figure 3.9, the 1/f corner frequency is 0.7Hz, and the white noise is 10nV/√Hz. The low frequency 1/f noise is often expressed as the peak-to-peak noise in the bandwidth 0.1Hz to 10Hz as shown in the scope photo in Figure 3.9. Note that this noise ultimately limits the resolution of a precision measurement system because the bandwidth up to 10Hz is usually the bandwidth of most interest. The equation for the total rms noise, $V_{n,rms}$, in the bandwidth F_L to F_H is given by the equation:

$$V_{n,rms}(F_H, F_L) = v_{nw}\sqrt{F_C \ln\left[\frac{F_H}{F_L}\right] + (F_H - F_L)},$$

where v_{nw} is the noise spectral density in the "white noise" region (usually specified at a frequency of 1kHz), F_C is the 1/f corner frequency, and F_L and F_H is the measurement bandwidth of interest. In the example shown, the 0.1Hz to 10Hz noise is calculated to be 36nV rms, or approximately 238nV peak-to-peak, which closely agrees with the scope photo on the right (a factor of 6.6 is generally used to convert rms values to peak-to-peak values).

It should be noted that at higher frequencies, the term in the equation containing the natural logarithm becomes insignificant, and the expression for the rms noise becomes:

$$V_{n,rms}(F_H, F_L) \approx v_{nw}\sqrt{F_H - F_L}\ .$$

And, if $F_H >> F_L$,

$$V_{n,rms}(F_H) \approx v_{nw}\sqrt{F_H}\ .$$

However, some op amps (such as the OP07 and OP27) have voltage noise characteristics that increase slightly at high frequencies. The voltage noise versus frequency curve for op amps should therefore be examined carefully for flatness when calculating high frequency noise using this approximation.

At very low frequencies when operating exclusively in the 1/f region, $F_C >> (F_H - F_L)$, and the expression for the rms noise reduces to:

$$V_{n,rms}(F_H, F_L) \approx v_{nw}\sqrt{F_C \ln\left[\frac{F_H}{F_L}\right]}\ .$$

Note that there is no way of reducing this 1/f noise by filtering if operation extends to DC. Making F_H=0.1Hz and F_L= 0.001 still yields an rms 1/f noise of about 18nV rms, or 119nV peak-to-peak.

The point is that averaging the results of a large number of measurements taken over a long period of time has practically no effect on the error produced by 1/f noise. The only method of reducing it further is to use a chopper stabilized op amp which does not pass the low frequency noise components.

A generalized noise model for an op amp is shown in Figure 3.10. All uncorrelated noise sources add as a root-sum-of-squares manner, i.e., noise voltages V1, V2, and V3 give a result of:

$$\sqrt{V1^2 + V2^2 + V3^2}\ .$$

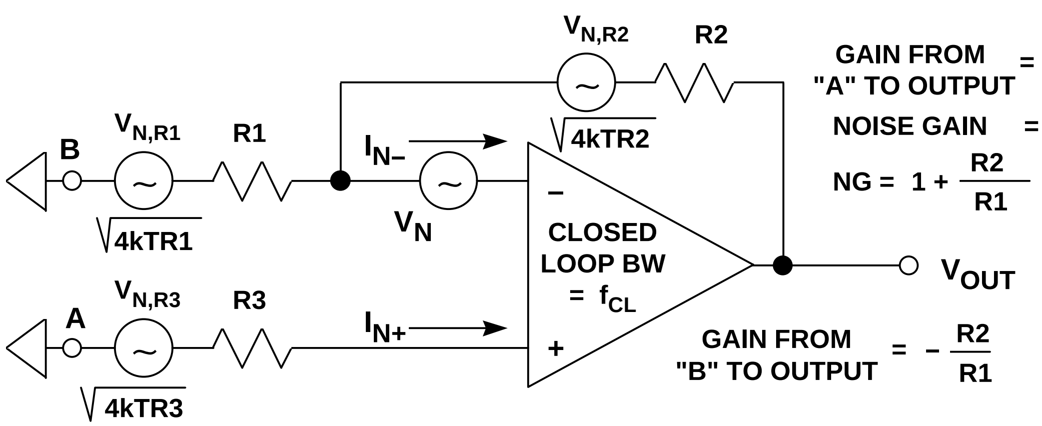
Thus, any noise voltage which is more than 4 or 5 times any of the others is dominant, and the others may generally be ignored. This simplifies noise analysis.

In this diagram, the total noise of all sources is shown referred to the input (RTI). The RTI noise is useful because it can be compared directly to the input signal level. The total noise referred to the output (RTO) is obtained by simply multiplying the RTI noise by the noise gain.

The diagram assumes that the feedback network is purely resistive. If it contains reactive elements (usually capacitors), the noise gain is not constant over the bandwidth of interest, and more complex techniques must be used to calculate the total noise (see in particular, Reference 12). However, for precision applications where the feedback network is most likely to be resistive, the equations are valid.

Notice that the Johnson noise voltage associated with the three resistors has been included. All resistors have a Johnson noise of $\sqrt{4kTBR}$, where k is Boltzmann's Constant (1.38×10^{-23} J/K), T is the absolute temperature, B is the bandwidth in Hz, and R is the resistance in Ω. A simple relationship which is easy to remember is that *a 1000*W*resistor generates a Johnson noise of 4nV/*Ö*Hz at 25°C.*

OP AMP NOISE MODEL



■ RTI NOISE =

$$\sqrt{BW} \bullet \sqrt{V_N^2 + 4kTR3 + 4kTR1\left[\frac{R2}{R1+R2}\right]^2 + I_{N+}^2R3^2 + I_{N-}^2\left[\frac{R1\bullet R2}{R1+R2}\right]^2 + 4kTR2\left[\frac{R1}{R1+R2}\right]^2}$$

■ RTO NOISE = NG • RTI NOISE

■ $BW = 1.57\ f_{CL}$

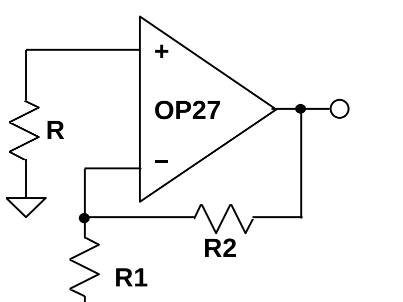
Figure 3.10

The voltage noise of various op amps may vary from under 1nV/√Hz to 20nV/√Hz, or even more. Bipolar input op amps tend to have lower voltage noise than JFET input ones, although it is possible to make JFET input op amps with low voltage noise (such as the AD743/AD745), at the cost of large input devices and hence large (~20pF) input capacitance. Current noise can vary much more widely, from around 0.1fA/√Hz (in JFET input electrometer op amps) to several pA/√Hz (in high speed bipolar op amps). For bipolar or JFET input devices where all the bias current flows into the input junction, the current noise is simply the Schottky (or shot) noise of the bias current. The shot noise spectral density is simply $\sqrt{2I_Bq}$ amps/√Hz, where I_B is the bias current (in amps) and q is the charge on an electron (1.6×10^{-19} C). It cannot be calculated for bias-compensated or current feedback op amps where the external bias current is the difference between two internal current sources.

Current noise is only important when it flows through an impedance and in turn generates a noise voltage. The equation shown in Figure 3.10 shows how the current noise flowing in the resistors contribute to the total noise. The choice of a low noise op amp therefore depends on the impedances around it. Consider an OP27, a bias compensated op amp with low voltage noise (3nV/√Hz), but quite high current noise (1pA/√Hz) as shown in the schematic of Figure 3.11. With zero source impedance, the voltage noise dominates. With a source resistance of 3kΩ, the current noise (1pA/√Hz) flowing in 3kΩ will equal the voltage noise, but the Johnson noise of the 3kΩ resistor is 7nV/√Hz and so is dominant. With a source resistance of 300kΩ, the effect of the current noise increases a hundredfold to 300nV/√Hz, while the voltage noise is unchanged, and the Johnson noise (which is proportional to the *square root* of the resistance) increases tenfold. Here, the current noise dominates.

DIFFERENT NOISE SOURCES DOMINATE AT DIFFERENT SOURCE IMPEDANCES

EXAMPLE: OP27
Voltage Noise = 3nV / √ Hz
Current Noise = 1pA / √ Hz
T = 25°C



Neglect R1 and R2 Noise Contribution

CONTRIBUTION FROM	VALUES OF R		
	0	3kΩ	300kΩ
AMPLIFIER VOLTAGE NOISE	**3**	3	3
AMPLIFIER CURRENT NOISE FLOWING IN R	0	3	**300**
JOHNSON NOISE OF R	0	**7**	70

RTI NOISE (nV / √ Hz)
Dominant Noise Source is Highlighted

Figure 3.11

The above example shows that the choice of a low noise op amp depends on the source impedance of the input signal, and at high impedances, current noise always dominates. This is shown in Figure 3.12 for several bipolar (OP07, OP27, 741) and JFET (AD645, AD743, AD744) op amps.

For low impedance circuitry (generally < 1kΩ), amplifiers with low voltage noise, such as the OP27 will be the obvious choice, and their comparatively large current noise will not affect the application. At medium resistances, the Johnson noise of resistors is dominant, while at very high resistances, we must choose an op amp with the smallest possible current noise, such as the AD549 or AD645.

Until recently, BiFET amplifiers (with JFET inputs) tended to have comparatively high voltage noise (though very low current noise), and thus were more suitable for low noise applications in high rather than low impedance circuitry. The AD645, AD743, and AD745 have very low values of both voltage and current noise. The AD645 specifications at 10kHz are 10nV/√Hz and 0.6fA/√Hz, and the AD743/AD745 specifications at 10kHz are 2.0nV/√Hz and 6.9fA/√Hz. These make possible the design of low noise amplifier circuits which have low noise over a wide range of source impedances.

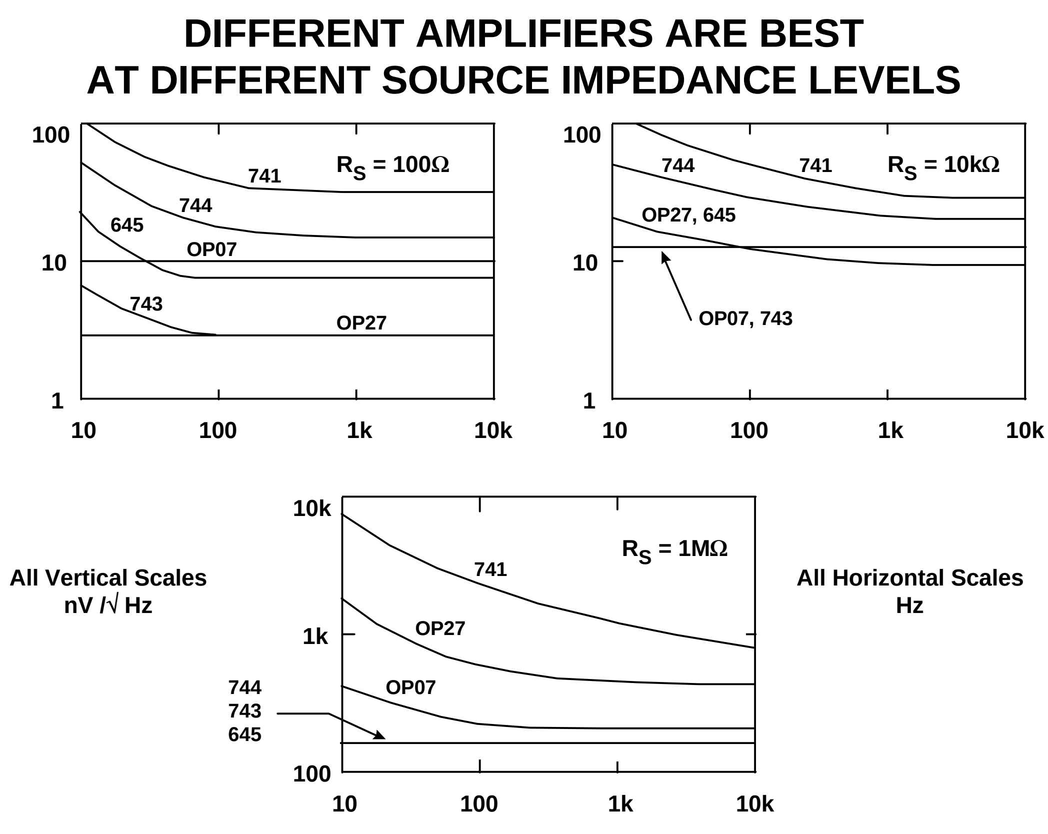


Figure 3.12

Common Mode Rejection and Power Supply Rejection

If a signal is applied equally to both inputs of an op amp so that the differential input voltage is unaffected, the output should not be affected. In practice, changes in common mode voltage will produce changes in the output. The *common mode rejection ratio* or CMRR is the ratio of the common mode gain to the differential-mode gain of an op amp. For example, if a differential input change of Y volts will produce a change of 1V at the output, and a common mode change of X volts produces a similar change of 1V, then the CMRR is X/Y. It is normally expressed in dB, and typical LF values are between 70 and 120dB. When expressed in dB, it is generally referred to as *common mode rejection* (CMR). At higher frequencies, CMR deteriorates - many op amp data sheets show a plot of CMR versus frequency as shown in Figure 3.13 for the OP177/AD707 precision op amps.

CMRR produces a corresponding output offset voltage error in op amps configured in the non-inverting mode as shown in Figure 3.14. Op amps configured in the inverting mode have no CMRR output error because both inputs are at ground or virtual ground, so there is no common mode voltage, only the offset voltage of the amplifier if un-nulled.

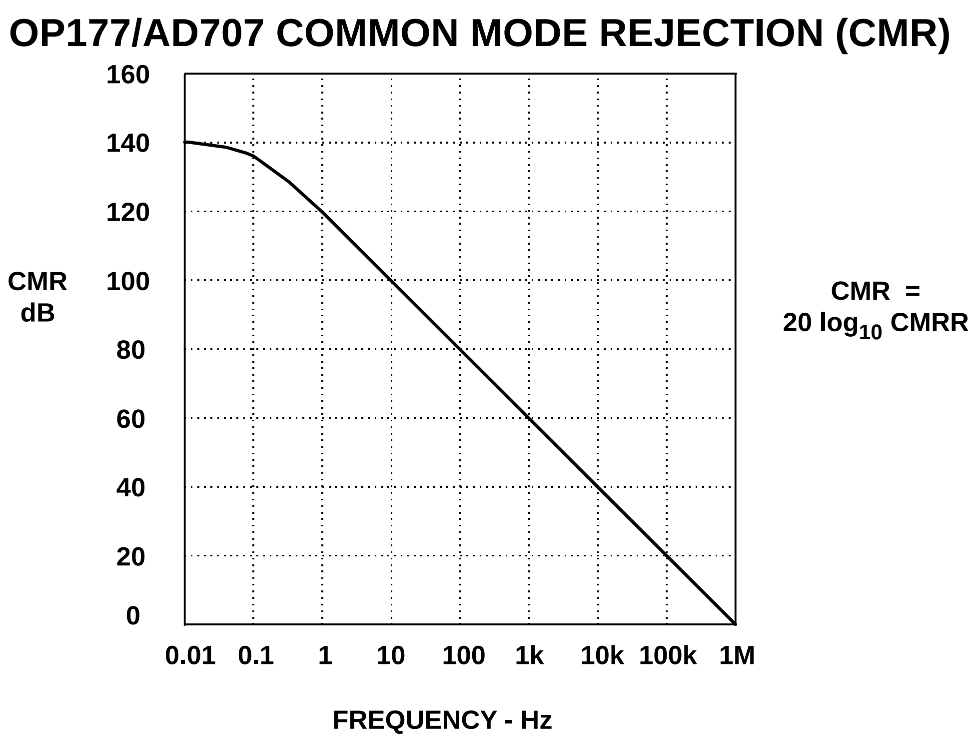
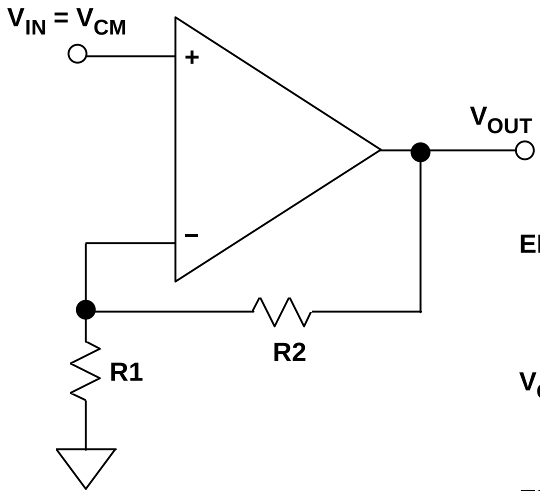


Figure 3.13

CALCULATING OFFSET ERROR DUE TO COMMON MODE REJECTION RATIO (CMRR)



$$\text{ERROR (RTI)} = \frac{V_{CM}}{\text{CMRR}} = \frac{V_{IN}}{\text{CMRR}}$$

$$V_{OUT} = \left[1 + \frac{R2}{R1}\right]\left[V_{IN} + \frac{V_{IN}}{\text{CMRR}}\right]$$

$$\text{ERROR (RTO)} = \left[1 + \frac{R2}{R1}\right]\left[\frac{V_{IN}}{\text{CMRR}}\right]$$

Figure 3.14

If the supply of an op amp changes, its output should not, but it will. The specification of *power supply rejection ratio* or PSRR is defined similarly to the definition of CMRR. If a change of X volts in the supply produces the same output change as a differential input change of Y volts, then the PSRR on that supply is X/Y. When the ratio is expressed in dB, it is generally referred to as *power supply rejection*, or PSR. The definition of PSRR assumes that both supplies are altered equally in opposite directions - otherwise the change will introduce a common mode change as well as a supply change, and the analysis becomes considerably more complex. It is this effect which causes apparent differences in PSRR between the positive and negative supplies. In the case of single supply op amps, PSR is generally defined with respect to the change in the positive supply. Many single supply op amps have separate PSR specifications for the positive and negative supplies. The PSR of the OP177/AD707 is shown in Figure 3.15.

The PSRR of op amps is frequency dependent, therefore power supplies must be well decoupled as shown in Figure 3.16. At low frequencies, several devices may share a 10 - 50µF capacitor on each supply, provided it is no more than 10cm (PC track distance) from any of them. At high frequencies, each IC must have every supply decoupled by a low inductance capacitor (0.1µF or so) with short leads and PC tracks. These capacitors must also provide a return path for HF currents in the op amp load. Decoupling capacitors should be connected to a low impedance large area ground plane with minimum lead lengths. Surface mount capacitors minimize lead inductance and are a good choice.

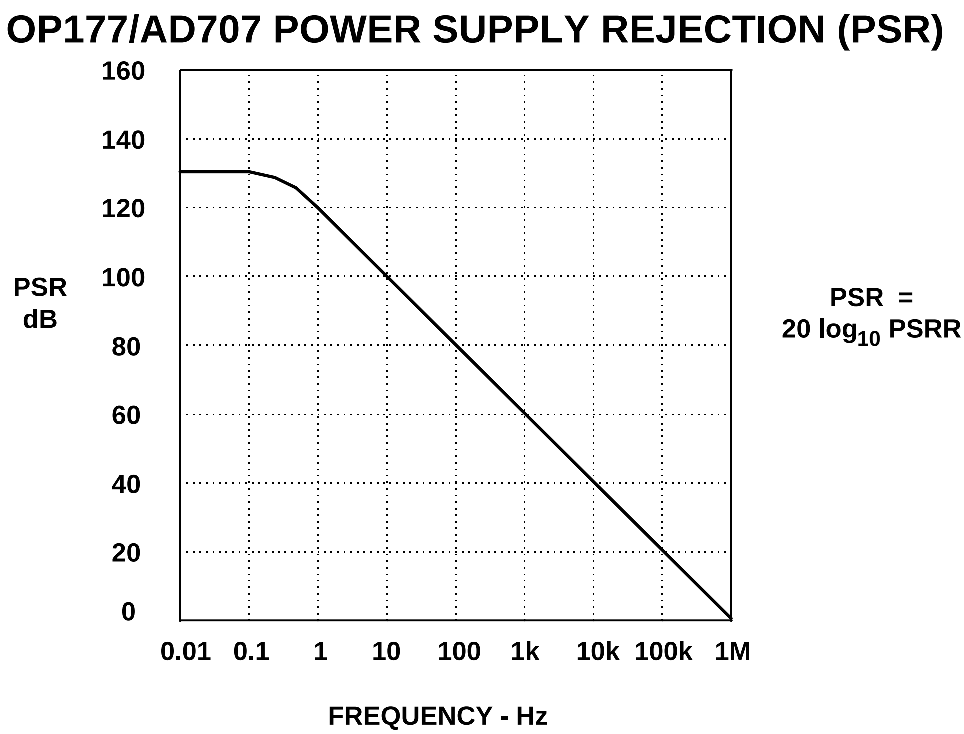


Figure 3.15

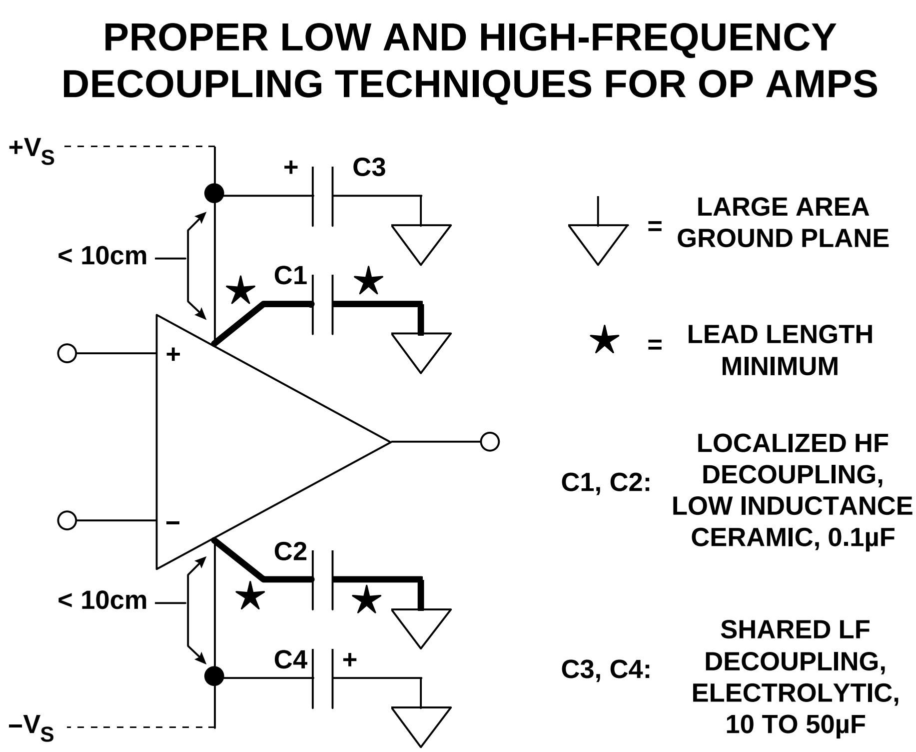


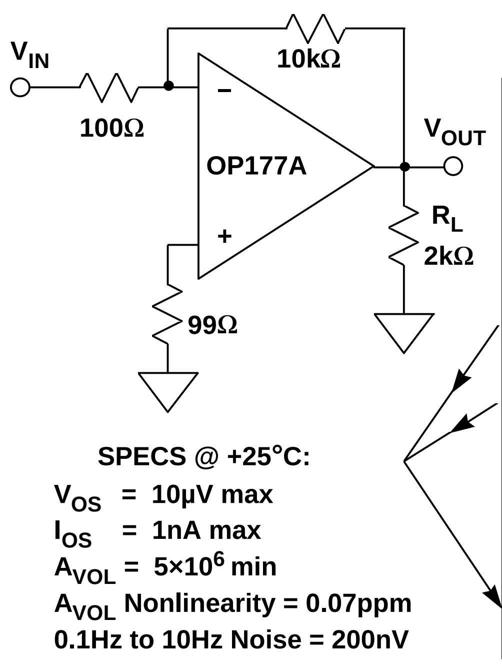
Figure 3.16

AMPLIFIER DC ERROR BUDGET ANALYSIS

A room temperature error budget analysis for the OP177A op amp is shown in Figure 3.17. The amplifier is connected in the inverting mode with a signal gain of 100. The key data sheet specifications are also shown in the diagram. We assume an input signal of 100mV fullscale which corresponds to an output signal of 10V. The various error sources are normalized to fullscale and expressed in parts per million (ppm). Note: parts per million (ppm) error = fractional error × 10^6 = % error × 10^4.

Note that the offset errors due to V_{OS} and I_{OS} and the gain error due to finite A_{VOL} can be removed with a system calibration. However, the error due to open loop gain nonlinearity cannot be removed with calibration and produces a relative accuracy error, often called *resolution error*. The second contributor to resolution error is the 1/f noise. This noise is always present and adds to the uncertainty of the measurement. The overall relative accuracy of the circuit at room temperature is 9ppm which is equivalent to approximately 17 bits of resolution.

PRECISION OP AMP (OP177A) DC ERROR BUDGET



MAXIMUM ERROR CONTRIBUTION, + 25°C
FULLSCALE: V_{IN}=100mV, V_{OUT} = 10V

V_{OS}	10µV ÷ 100mV	100ppm
I_{OS}	100Ω × 1nA ÷ 100mV	1ppm
A_{VOL}	(100/ 5×10^6) × 100mV	20ppm
A_{VOL} Nonlinearity	100 × 0.07ppm	7ppm
0.1Hz to 10Hz 1/f Noise	200nV ÷ 100mV	2ppm
Total Unadjusted Error	≈ 13 Bits Accurate	130ppm
Resolution Error	≈ 17 Bits Accurate	9ppm

Figure 3.17

SINGLE SUPPLY OP AMPS

Over the last several years, single-supply operation has become an increasingly important requirement because of market requirements. Automotive, set-top box, camera/cam-corder, PC, and laptop computer applications are demanding IC vendors to supply an array of linear devices that operate on a single supply rail, with the same performance of dual supply parts. Power consumption is now a key parameter for line or battery operated systems, and in some instances, more important than cost. This makes low-voltage/low supply current operation critical; at the same time, however, accuracy and precision requirements have forced IC manufacturers to meet the challenge of "doing more with less" in their amplifier designs.

SINGLE SUPPLY AMPLIFIERS

- **Single Supply Offers:**
  - **Lower Power**
  - **Battery Operated Portable Equipment**
  - **Requires Only One Voltage**
- **Design Tradeoffs:**
  - **Reduced Signal Swing Increases Sensitivity to Errors Caused by Offset Voltage, Bias Current, Finite Open-Loop Gain, Noise, etc.**
  - **Must Usually Share Noisy Digital Supply**
  - **Rail-to-Rail Input and Output Needed to Increase Signal Swing**
  - **Precision Less than the best Dual Supply Op Amps but not Required for All Applications**
  - **Many Op Amps Specified for Single Supply, but do not have Rail-to-Rail Inputs or Outputs**

Figure 3.18

In a single-supply application, the most immediate effect on the performance of an amplifier is the reduced input and output signal range. As a result of these lower input and output signal excursions, amplifier circuits become more sensitive to internal and external error sources. Precision amplifier offset voltages on the order of 0.1mV are less than a 0.04 LSB error source in a 12-bit, 10V full-scale system. In a single-supply system, however, a "rail-to-rail" precision amplifier with an offset voltage of 1mV represents a 0.8LSB error in a 5V fullscale system, and 1.6LSB error in a 2.5V fullscale system.

To keep battery current drain low, larger resistors are usually used around the op amp. Since the bias current flows through these larger resistors, they can generate offset errors equal to or greater than the amplifier's own offset voltage.

Gain accuracy in some low voltage single-supply devices is also reduced, so device selection needs careful consideration. Many amplifiers having open-loop gains in the millions typically operate on dual supplies: for example, the OP07 family types. However, many single-supply/rail-to-rail amplifiers for precision applications typically have open-loop gains between 25,000 and 30,000 under light loading (>10kΩ). Selected devices, like the OP113/213/413 family, do have high open-loop gains (i.e., > 1M).

Many trade-offs are possible in the design of a single-supply amplifier circuit: speed versus power, noise versus power, precision versus speed and power, etc. Even if the noise floor remains constant (highly unlikely), the signal-to-noise ratio will drop as the signal amplitude decreases.

Besides these limitations, many other design considerations that are otherwise minor issues in dual-supply amplifiers now become important. For example, signal-to-noise (SNR) performance degrades as a result of reduced signal swing. "Ground reference" is no longer a simple choice, as one reference voltage may work for some devices, but not others. Amplifier voltage noise increases as operating supply current drops, and bandwidth decreases. Achieving adequate bandwidth and required precision with a somewhat limited selection of amplifiers presents significant system design challenges in single-supply, low-power applications.

Most circuit designers take "ground" reference for granted. Many analog circuits scale their input and output ranges about a ground reference. In dual-supply applications, a reference that splits the supplies (0V) is very convenient, as there is equal supply headroom in each direction, and 0V is generally the voltage on the low impedance ground plane.

In single-supply/rail-to-rail circuits, however, the ground reference can be chosen anywhere within the supply range of the circuit, since there is no standard to follow. The choice of ground reference depends on the type of signals processed and the amplifier characteristics. For example, choosing the negative rail as the ground reference may optimize the dynamic range of an op amp whose output is designed to swing to 0V. On the other hand, the signal may require level shifting in order to be compatible with the input of other devices (such as ADCs) that are not designed to operate at 0V input.

Early single-supply "zero-in, zero-out" amplifiers were designed on bipolar processes which optimized the performance of the NPN transistors. The PNP transistors were either lateral or substrate PNPs with much less bandwidth than the NPNs. Fully complementary processes are now required for the new-breed of single-supply/rail-to-rail operational amplifiers. These new amplifier designs do not use lateral or substrate PNP transistors within the signal path, but incorporate parallel NPN and PNP input stages to accommodate input signal swings from ground to the positive supply rail. Furthermore, rail-to-rail output stages are designed with bipolar NPN and PNP common-emitter, or N-channel/P-channel common-source amplifiers whose

collector-emitter saturation voltage or drain-source channel on-resistance determine output signal swing as a function of the load current.

The characteristics of a single-supply amplifier input stage (common mode rejection, input offset voltage and its temperature coefficient, and noise) are critical in precision, low-voltage applications. Rail-to-rail input operational amplifiers must resolve small signals, whether their inputs are at ground, or in some cases near the amplifier's positive supply. Amplifiers having a minimum of 60dB common mode rejection over the entire input common mode voltage range from 0V to the positive supply are good candidates. It is not necessary that amplifiers maintain common mode rejection for signals beyond the supply voltages: *what is required is that they do not self-destruct for momentary overvoltage conditions*. Furthermore, amplifiers that have offset voltages less than 1mV and offset voltage drifts less than 2µV/°C are also very good candidates for precision applications. Since *input* signal dynamic range and SNR are equally if not more important than *output* dynamic range and SNR, precision single-supply/rail-to-rail operational amplifiers should have noise levels referred-to-input (RTI) less than 5µVp-p in the 0.1Hz to 10Hz band.

The need for rail-to-rail amplifier output stages is driven by the need to maintain wide dynamic range in low-supply voltage applications. A single-supply/rail-to-rail amplifier should have output voltage swings which are within at least 100mV of either supply rail (under a nominal load). The output voltage swing is very dependent on output stage topology and load current. The voltage swing of a good output stage should maintain its rated swing for loads down to 10kΩ. The smaller the V_{OL} and the larger the V_{OH}, the better. System parameters, such as "zero-scale" or "full-scale" output voltage, should be determined by an amplifier's V_{OL} (for zero-scale) and V_{OH} (for full-scale).

Since the majority of single-supply data acquisition systems require at least 12- to 14-bit performance, amplifiers which exhibit an open-loop gain greater than 30,000 for all loading conditions are good choices in precision applications.

Single Supply Op Amp Input Stages

There is some demand for op amps whose input common mode voltage includes *both* supply rails. Such a feature is undoubtedly useful in some applications, but engineers should recognize that there are relatively few applications where it is absolutely essential. These should be carefully distinguished from the many applications where common mode range *close* to the supplies or one that includes *one* of the supplies is necessary, but input rail-to-rail operation is not.

In many single-supply applications, it is required that the input go to only one of the supply rails (usually ground). High-side or low-side sensing applications are good examples of this. Amplifiers which will handle zero-volt inputs are relatively easily designed using PNP differential pairs (or N-channel JFET pairs) as shown in Figure 3.19. The input common mode range of such an op amp extends from about 200mV below the negative supply to within about 1V of the positive supply.

PNP OR N-CHANNEL JFET STAGES ALLOW INPUT SIGNAL TO GO TO THE NEGATIVE RAIL

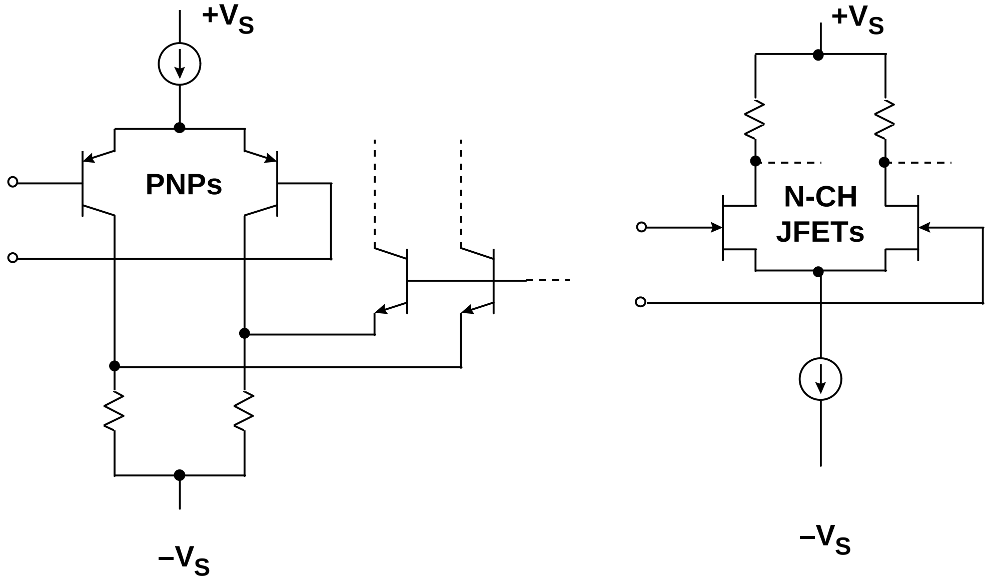


Figure 3.19

The input stage could also be designed with NPN transistors (or P-channel JFETs), in which case the input common mode range would include the positive rail and to within about 1V of the negative rail. This requirement typically occurs in applications such as high-side current sensing, a low-frequency measurement application. The OP282/OP482 input stage uses the P-channel JFET input pair whose input common mode range includes the positive rail. Other circuit topologies for high-side sensing (such as the AD626) use the precision resistors to attenuate the common mode voltage.

True rail-to-rail input stages require two long-tailed pairs (see Figure 3.20), one of NPN bipolar transistors (or N-channel JFETs), the other of PNP transistors (or P-channel JFETs). These two pairs exhibit *different* offsets and bias currents, so when the applied input common mode voltage changes, the amplifier input offset voltage and input bias current does also. In fact, when both current sources remain active throughout the entire input common mode range, amplifier input offset voltage is the *average* offset voltage of the NPN pair and the PNP pair. In those designs where the current sources are alternatively switched off at some point along the input common mode voltage, amplifier input offset voltage is dominated by the PNP pair offset voltage for signals near the negative supply, and by the NPN pair offset voltage for signals near the positive supply. It should be noted that true rail-to-rail input stages can also be constructed from CMOS transistors as in the case of the OP250/450 and the AD8531/8532/8534.

TRUE RAIL-TO-RAIL INPUT STAGE

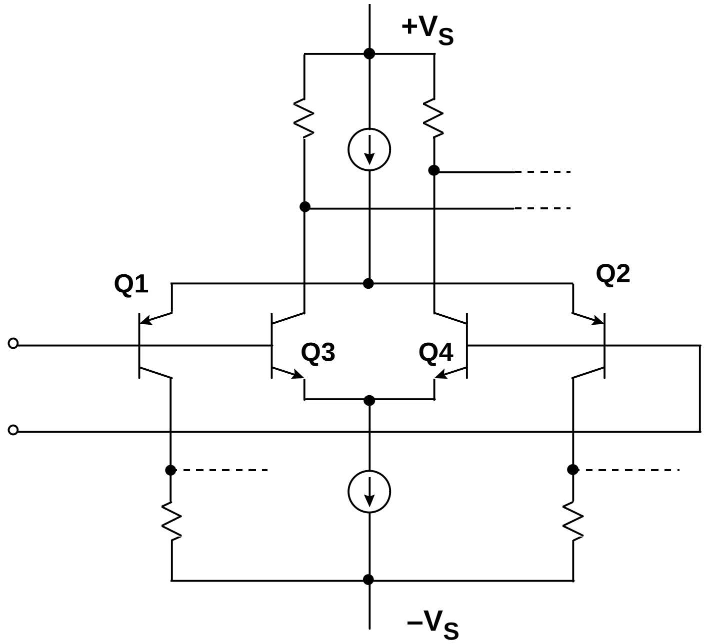


Figure 3.20

Amplifier input bias current, a function of transistor current gain, is also a function of the applied input common mode voltage. The result is relatively poor common mode rejection (CMR), and a changing common mode input impedance over the common mode input voltage range, compared to familiar dual-supply devices. These specifications should be considered carefully when choosing a rail-rail input op amp, especially for a non-inverting configuration. Input offset voltage, input bias current, and even CMR may be quite good over *part* of the common mode range, but much worse in the region where operation shifts between the NPN and PNP devices and vice versa.

True rail-to-rail amplifier input stage designs must transition from one differential pair to the other differential pair somewhere along the input common mode voltage range. Some devices like the OP191/291/491 family and the OP279 have a common mode crossover threshold at approximately 1V below the positive supply. The PNP differential input stage is active from about 200mV below the negative supply to within about 1V of the positive supply. Over this common mode range, amplifier input offset voltage, input bias current, CMR, input noise voltage/current are primarily determined by the characteristics of the PNP differential pair. At the crossover threshold, however, amplifier input offset voltage becomes the average offset voltage of the NPN/PNP pairs and can change rapidly. Also, amplifier bias currents, dominated by the PNP differential pair over most of the input common mode range, change polarity and magnitude at the crossover threshold when the NPN differential pair becomes active.

Op amps like the OP184/284/484, utilize a rail-to-rail input stage design where both NPN and PNP transistor pairs are active throughout the entire input common mode voltage range, and there is no common mode crossover threshold. Amplifier input offset voltage is the average offset voltage of the NPN and the PNP stages. Amplifier

input offset voltage exhibits a smooth transition throughout the entire input common mode range because of careful laser trimming of the resistors in the input stage. In the same manner, through careful input stage current balancing and input transistor design, amplifier input bias currents also exhibit a smooth transition throughout the entire common mode input voltage range. The exception occurs at the extremes of the input common mode range, where amplifier offset voltages and bias currents increase sharply due to the slight forward-biasing of parasitic p-n junctions. This occurs for input voltages within approximately 1V of either supply rail.

When *both* differential pairs are active throughout the entire input common mode range, amplifier transient response is faster through the middle of the common mode range by as much as a factor of 2 for bipolar input stages and by a factor of $\sqrt{2}$ for JFET input stages. Input stage transconductance determines the slew rate and the unity-gain crossover frequency of the amplifier, hence response time degrades slightly at the extremes of the input common mode range when either the PNP stage (signals approaching the positive supply rail) or the NPN stage (signals approaching the negative supply rail) are forced into cutoff. The thresholds at which the transconductance changes occur are approximately within 1V of either supply rail, and the behavior is similar to that of the input bias currents.

Applications which require true rail-rail inputs should therefore be carefully evaluated, and the amplifier chosen to ensure that its input offset voltage, input bias current, common mode rejection, and noise (voltage and current) are suitable.

Single Supply Op Amp Output Stages

The earliest IC op amp output stages were NPN emitter followers with NPN current sources or resistive pull-downs, as shown in the left-hand diagram of Figure 3.21. Naturally, the slew rates were greater for positive-going than for negative-going signals. While all modern op amps have push-pull output stages of some sort, many are still asymmetrical, and have a greater slew rate in one direction than the other. Asymmetry tends to introduce distortion on AC signals and generally results from the use of IC processes with faster NPN than PNP transistors. It may also result in the ability of the output to approach one supply more closely than the other.

In many applications, the output is required to swing only to one rail, usually the negative rail (i.e., ground in single-supply systems). A pulldown resistor to the negative rail will allow the output to approach that rail (provided the load impedance is high enough, or is also grounded to that rail), but only slowly. Using an FET current source instead of a resistor can speed things up, but this adds complexity.

With new complementary bipolar processes (CB), well matched high speed PNP and NPN transistors are available. The complementary emitter follower output stage shown in the right-hand diagram of Figure 3.21 has many advantages including low output impedance. However, the output can only swing within about one V_{BE} drop of either supply rail. An output swing of +1V to +4V is typical of such stages when operated on a single +5V supply.

TRADITIONAL OUTPUT STAGES

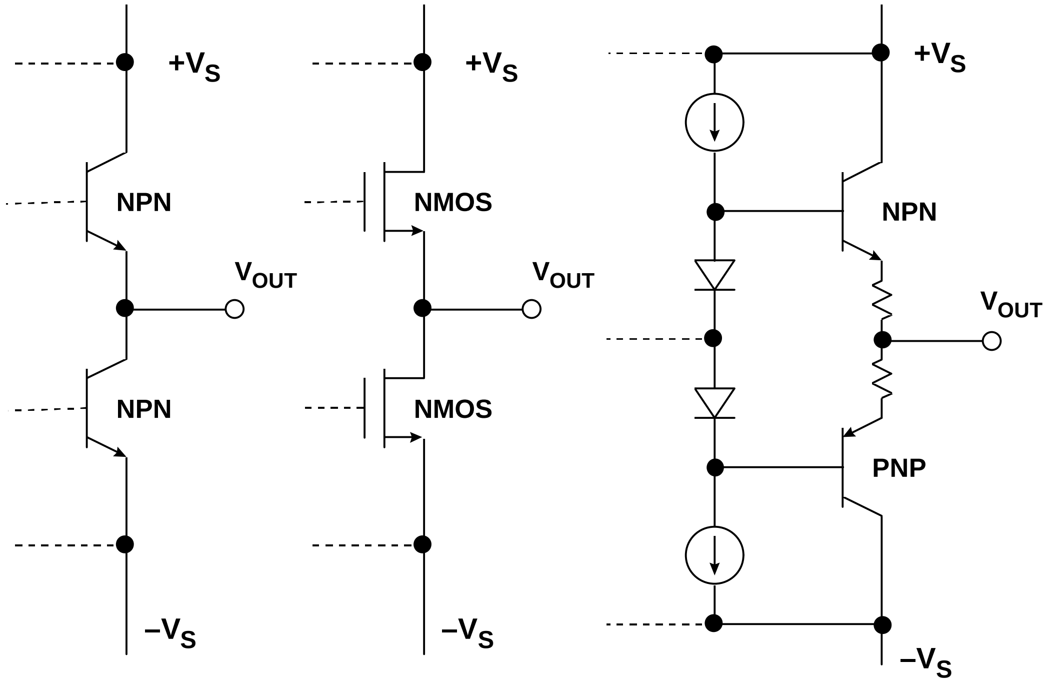


Figure 3.21

The complementary common-emitter/common-source output stages shown in Figure 3.22 allow the output voltage to swing much closer to the output rails, but these stages have higher open loop output impedance than the emitter follower- based stages. In practice, however, the amplifier's open loop gain and local feedback produce an apparent low output impedance, particularly at frequencies below 10Hz.

The complementary common emitter output stage using BJTs (left-hand diagram in Figure 3.22) cannot swing completely to the rails, but only to within the transistor saturation voltage (V_{CESAT}) of the rails. For small amounts of load current (less than 100µA), the saturation voltage may be as low as 5 to 10mV, but for higher load currents, the saturation voltage can increase to several hundred mV (for example, 500mV at 50mA).

On the other hand, an output stage constructed of CMOS FETs can provide nearly true rail-to-rail performance, but only under no-load conditions. If the output must source or sink current, the output swing is reduced by the voltage dropped across the FETs internal "on" resistance (typically, 100Ω for precision amplifiers, but can be less than 10Ω for high current drive CMOS amplifiers).

For these reasons, it is apparent that there is no such thing as a true rail-to-rail output stage, hence the title of Figure 3.22 ("Almost" Rail-to-Rail Output Stages).

"ALMOST" RAIL-TO-RAIL OUTPUT STRUCTURES

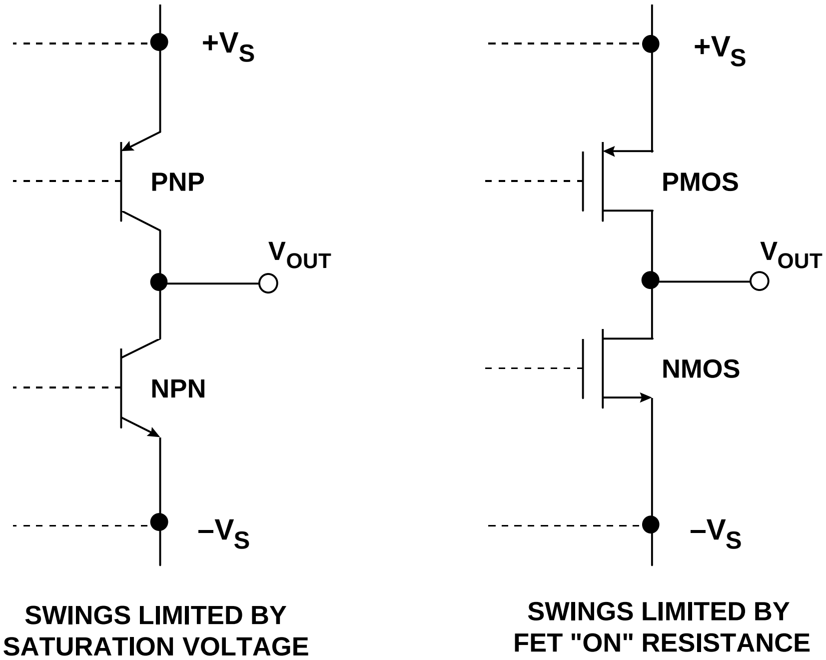


Figure 3.22

Figure 3.23 summarizes the performance characteristics of a number of single-supply op amps suitable for some precision applications. The devices are listed in order of increasing supply current. Single, dual, and quad versions of each op amp are available, so the supply current is the normalized I_{SY}/amplifier for comparison. The input and output voltage ranges (V_S = +5V) are also supplied in the table. The "0, 4V" inputs are PNP pairs, with the exception of the AD820/822/824 which use N-Channel JFETs. Output stages having voltage ranges designated "5mV, 4V" are NPN emitter-followers with current source pull-downs (OP193/293/493, OP113/213/413). Output stages designated "R/R" use CMOS common source stages (OP181/281/481) or CB common emitter stages (OP196/296/496, OP191/291/491, AD820/822/824, OP184/284/484).

In summary, the following points should be considered when selecting amplifiers for single-supply/rail-to-rail applications:

First, input offset voltage and input bias currents are a function of the applied input common mode voltage (for true rail-to-rail input op amps). Circuits using this class of amplifiers should be designed to minimize resulting errors. An inverting amplifier configuration with a false ground reference at the non-inverting input prevents these errors by holding the input common mode voltage constant. If the inverting amplifier configuration cannot be used, then amplifiers like the OP184/284/OP484 which do not exhibit any common mode crossover thresholds should be used.

PRECISION SINGLE-SUPPLY OP AMP PERFORMANCE CHARACTERISTICS

****LISTED IN ORDER OF INCREASING SUPPLY CURRENT**

**PART NO.	V_{OS} max	V_{OS} TC	A_{VOL}min	NOISE (1kHz)	INPUT	OUTPUT	I_{SY}/AMP
OP181/281/481	1500µV	10µV/°C	5M	70nV/√Hz	0, 4V	"R/R"	4µA
OP193/293/493	75µV	0.2µV/°C	200k	65nV/√Hz	0, 4V	5mV, 4V	15µA
OP196/296/496	300µV	1.5µV/°C	150k	26nV/√Hz	R/R	"R/R"	50µA
OP191/291/491	700µV	1.1µV/°C	25k	35nV/√Hz	R/R	"R/R"	400µA
*AD820/822/824	400µV	2µV/°C	500k	16nV/√Hz	0, 4V	"R/R"	800µA
OP184/284/484	65µV	0.2µV/°C	50k	3.9nV/√Hz	R/R	"R/R"	1250µA
OP113/213/413	125µV	0.2µV/°C	2M	4.7nV/√Hz	0, 4V	5mV, 4V	1750µA

*JFET INPUT

NOTE: Unless Otherwise Stated Specifications are Typical @ +25°C V_S = +5V

Figure 3.23

Second, since input bias currents are not always small and can exhibit different polarities, source impedance levels should be carefully matched to minimize additional input bias current-induced offset voltages and increased distortion. Again, consider using amplifiers that exhibit a smooth input bias current transition throughout the applied input common mode voltage.

Third, rail-to-rail amplifier output stages exhibit load-dependent gain which affects amplifier open-loop gain, and hence closed-loop gain accuracy. Amplifiers with open-loop gains greater than 30,000 for resistive loads less than 10kΩ are good choices in precision applications. For applications not requiring full rail-rail swings, device families like the OP113/213/413 and OP193/293/493 offer DC gains of 200,000 or more.

Lastly, no matter what claims are made, rail-to-rail output voltage swings are functions of the amplifier's output stage devices and load current. The saturation voltage (V_{CESAT}), saturation resistance (R_{SAT}) for bipolar output stages, and FET on-resistance for CMOS output stages, as well as load current all affect the amplifier output voltage swing.

Op Amp Process Technologies

The wide variety of processes used to make op amps are shown in Figure 3.24. The earliest op amps were made using standard NPN-based bipolar processes. The PNP transistors available on these processes were extremely slow and were used primarily for current sources and level shifting.

The ability to produce matching high speed PNP transistors on a bipolar process added great flexibility to op amp circuit designs. These complementary bipolar (CB) processes are widely used in today's precision op amps, as well as those requiring wide bandwidths. The high-speed PNP transistors have f_ts which are greater than one-half the f_ts of the NPNs.

The addition of JFETs to the complementary bipolar process (CBFET) allow high input impedance op amps to be designed suitable for such applications as photodiode or electrometer preamplifiers.

CMOS op amps, with a few exceptions, generally have relatively poor offset voltage, drift, and voltage noise. However, the input bias current is very low. They offer low power and cost, however, and improved performance can be achieved with BiFET or CBFET processes.

The addition of bipolar or complementary devices to a CMOS process (BiMOS or CBCMOS) adds great flexibility, better linearity, and low power. The bipolar devices are typically used for the input stage to provide good gain and linearity, and CMOS devices for the rail-to-rail output stage.

In summary, there is no single IC process which is optimum for all op amps. Process selection and the resulting op amp design depends on the targeted applications and ultimately should be transparent to the customer.

OP AMP PROCESS TECHNOLOGY SUMMARY

- **BIPOLAR (NPN-BASED): This is Where it All Started!!**
- **COMPLEMENTARY BIPOLAR (CB): Rail-to-Rail, Precision, High Speed**
- **BIPOLAR + JFET (BiFET): High Input Impedance, High Speed**
- **COMPLEMENTARY BIPOLAR + JFET (CBFET): High Input Impedance, Rail-to-Rail Output, High Speed**
- **COMPLEMENTARY MOSFET (CMOS): Low Cost, Non-Critical Op Amps**
- **BIPOLAR + CMOS (BiCMOS): Bipolar Input Stage adds Linearity, Low Power, Rail-to-Rail Output**
- **COMPLEMENTARY BIPOLAR + CMOS (CBCMOS): Rail-to-Rail Inputs, Rail-to-Rail Outputs, Good Linearity, Low Power**

Figure 3.24

INSTRUMENTATION AMPLIFIERS (IN-AMPS)

An instrumentation amplifier is a closed-loop gain block which has a differential input and an output which is single-ended with respect to a reference terminal (see Figure 3.25). The input impedances are balanced and have high values, typically $10^9\Omega$ or higher. Unlike an op amp, which has its closed-loop gain determined by external resistors connected between its inverting input and its output, an in-amp employs an internal feedback resistor network which is isolated from its signal input terminals. With the input signal applied across the two differential inputs, gain is either preset internally or is user-set by an internal (via pins) or external gain resistor, which is also isolated from the signal inputs. Typical in-amp gain settings range from 1 to 10,000.

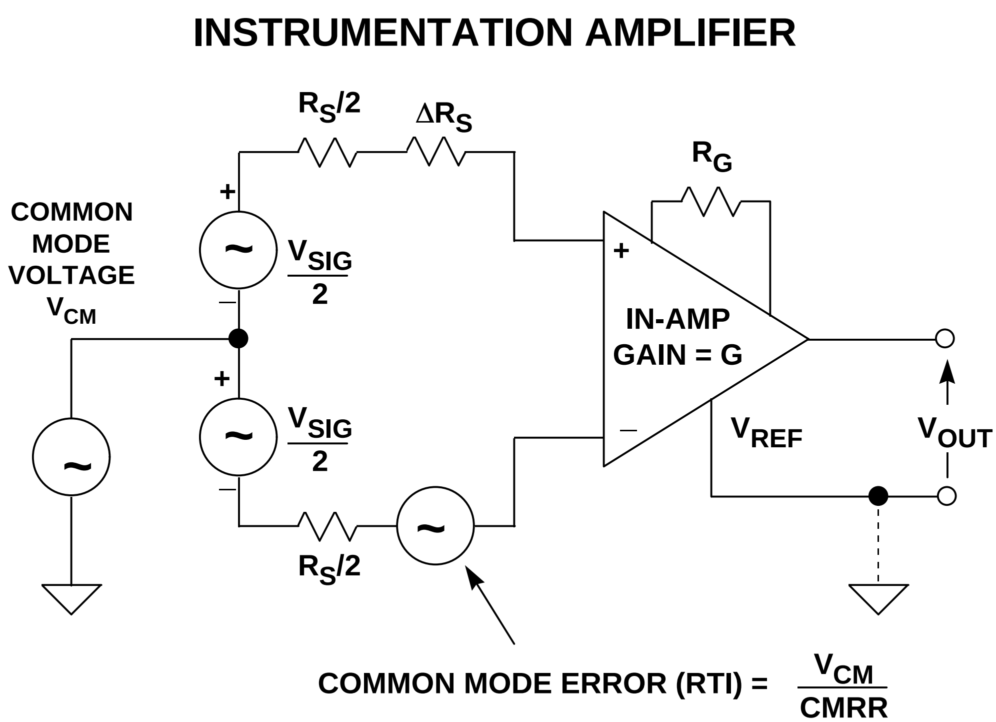


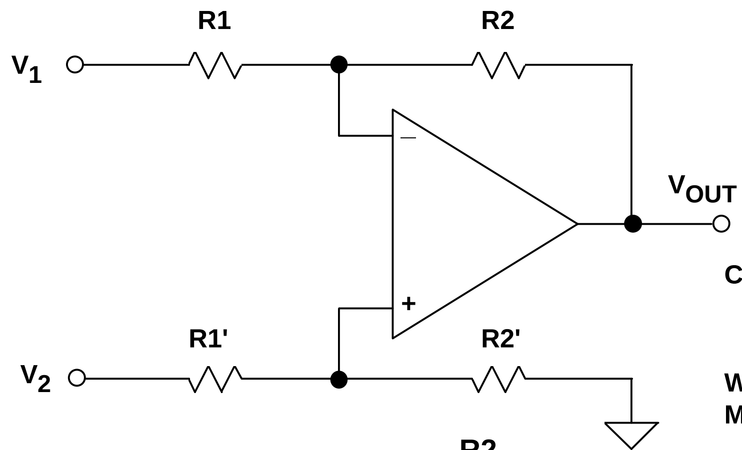
Figure 3.25

In order to be effective, an in-amp needs to be able to amplify microvolt-level signals, while simultaneously rejecting volts of common mode signal at its inputs. This requires that in-amps have very high common mode rejection (CMR): typical values of CMR are 70dB to over 100dB, with CMR usually improving at higher gains.

It is important to note that a CMR specification for DC inputs alone is not sufficient in most practical applications. In industrial applications, the most common cause of external interference is pickup from the 50/60Hz AC power mains. Harmonics of the power mains frequency can also be troublesome. In differential measurements, this type of interference tends to be induced equally onto both in-amp inputs. The interfering signal therefore appears as a common mode signal to the in-amp. Specifying CMR over frequency is more important than specifying its DC value. Imbalance in the source impedance can degrade the CMR of some in-amps. Analog Devices fully specifies in-amp CMR at 50/60Hz with a source impedance imbalance of 1kΩ.

Low-frequency CMR of op amps, connected as subtractors as shown in Figure 3.26, generally is a function of the resistors around the circuit, not the op amp. A mismatch of only 0.1% in the resistor ratios will reduce the DC CMR to approximately 66dB. Another problem with the simple op amp subtractor is that the input impedances are relatively low and are unbalanced between the two sides. The input impedance seen by V_1 is R_1, but the input impedance seen by V_2 is R1' + R2'. This configuration can be quite problematic in terms of CMR, since even a small source impedance imbalance (~ 10 Ω) will degrade the workable CMR.

OP AMP SUBTRACTOR



$$CMR = 20 \log_{10}\left[\frac{1 + \frac{R2}{R1}}{Kr}\right]$$

Where Kr = Total Fractional Mismatch of R1 - R2

- $V_{OUT} = (V_2 - V_1)\frac{R2}{R1}$
- $\frac{R2}{R1} = \frac{R2'}{R1'}$ CRITICAL FOR HIGH CMR
- EXTREMELY SENSITIVE TO SOURCE IMPEDANCE IMBALANCE
- 0.1% TOTAL MISMATCH YIELDS ≈ 66dB CMR FOR R1 = R2

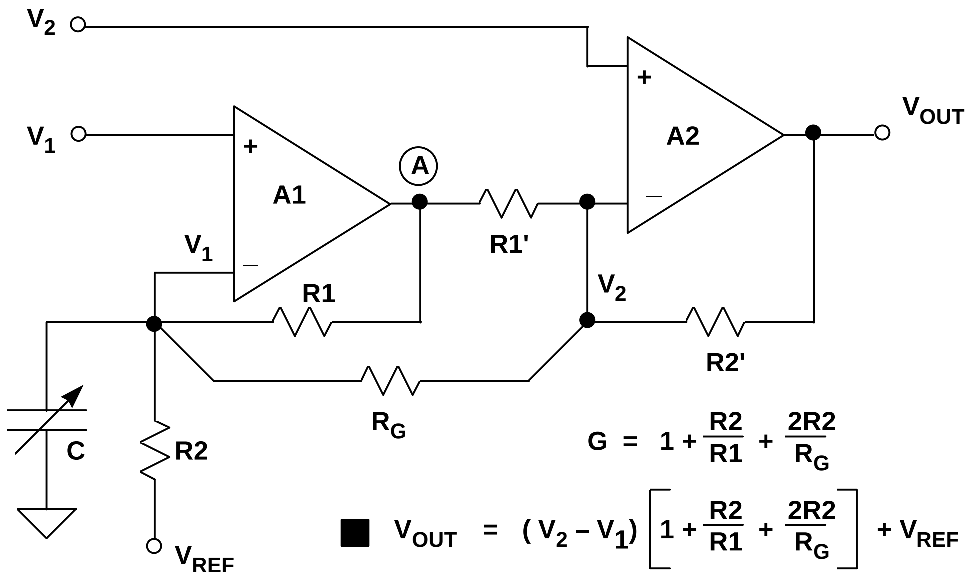
Figure 3.26

Instrumentation Amplifier Configurations

Instrumentation amplifier configurations are based on op amps, but the simple subtractor circuit described above lacks the performance required for precision applications. An in-amp architecture which overcomes some of the weaknesses of the subtractor circuit uses two op amps as shown in Figure 3.27. This circuit is typically referred to as the *two op amp in-amp*. Dual IC op amps are used in most cases for good matching. The circuit gain may be trimmed with an external resistor, R_G. The input impedance is high, permitting the impedance of the signal sources to be high and unbalanced. The DC common mode rejection is limited by the matching of R1/R2 to R1'/R2'. If there is a mismatch in any of the four resistors, the DC common mode rejection is limited to:

$$CMR \le 20 \log\left[\frac{GAIN \times 100}{\%MISMATCH}\right].$$

TWO OP AMP INSTRUMENTATION AMPLIFIER



$$G = 1 + \frac{R2}{R1} + \frac{2R2}{R_G}$$

- $V_{OUT} = (V_2 - V_1)\left[1 + \frac{R2}{R1} + \frac{2R2}{R_G}\right] + V_{REF}$
- $\frac{R2}{R1} = \frac{R2'}{R1'}$
- $CMR \leq 20\log\left[\frac{GAIN \times 100}{\%\ MISMATCH}\right]$

Figure 3.27

There is an implicit advantage to this configuration due to the gain executed on the signal. This raises the CMR in proportion.

Integrated instrumentation amplifiers are particularly well suited to meeting the combined needs of ratio matching and temperature tracking of the gain-setting resistors. While thin film resistors fabricated on silicon have an initial tolerance of up to ±20%, laser trimming during production allows the ratio error between the resistors to be reduced to 0.01% (100ppm). Furthermore, the tracking between the temperature coefficients of the thin film resistors is inherently low and is typically less than 3ppm/ºC (0.0003%/ºC).

When dual supplies are used, V_{REF} is normally connected directly to ground. In single supply applications, V_{REF} is usually connected to a low impedance voltage source equal to one-half the supply voltage. The gain from V_{REF} to node "A" is R1/R2, and the gain from node "A" to the output is R2'/R1'. This makes the gain from V_{REF} to the output equal to unity, assuming perfect ratio matching. Note that it is critical that the source impedance seen by V_{REF} be low, otherwise CMR will be degraded.

One major disadvantage of this design is that common mode voltage input range must be traded off against gain. The amplifier A1 must amplify the signal at V_1 by

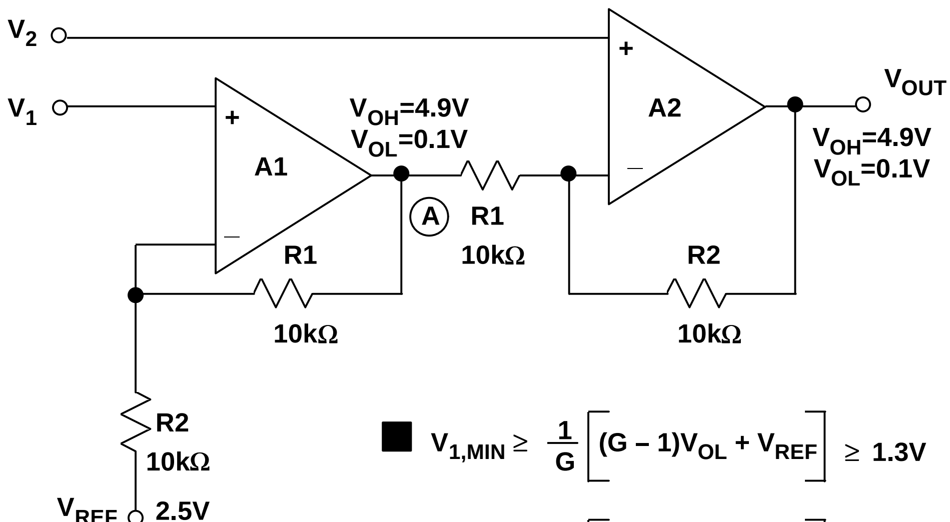
$$1 + \frac{R1}{R2}.$$

If R1 >> R2 (low gain in Figure 3.27), A1 will saturate if the common mode signal is too high, leaving no headroom to amplify the wanted differential signal. For high gains (R1<< R2), there is correspondingly more headroom at node "A" allowing larger common mode input voltages.

The AC common mode rejection of this configuration is generally poor because the signal from V_1 to V_{OUT} has the additional phase shift of A1. In addition, the two amplifiers are operating at different closed-loop gains (and thus at different bandwidths). The use of a small trim capacitor "C" as shown in the diagram can improve the AC CMR somewhat.

A low gain (G = 2) single supply two op amp in-amp configuration results when R_G is not used, and is shown in Figure 3.28. The input common mode and differential signals must be limited to values which prevent saturation of either A1 or A2. In the example, the op amps remain linear to within 0.1V of the supply rails, and their upper and lower output limits are designated V_{OH} and V_{OL}, respectively. Using the equations shown in the diagram, the voltage at V_1 must fall between 1.3V and 2.4V to prevent A1 from saturating. Notice that V_{REF} is connected to the average of V_{OH} and V_{OL} (2.5V). This allows for bipolar differential input signals with V_{OUT} referenced to +2.5V.

SINGLE SUPPLY RESTRICTIONS: V_S = +5V, G = 2



$$V_{REF} = \frac{V_{OH} + V_{OL}}{2} = 2.5V$$

- $V_{1,MIN} \geq \frac{1}{G}\left[(G-1)V_{OL} + V_{REF}\right] \geq 1.3V$
- $V_{1,MAX} \leq \frac{1}{G}\left[(G-1)V_{OH} + V_{REF}\right] \leq 3.7V$
- $\left|V_2 - V_1\right|_{MAX} \leq \frac{V_{OH} - V_{OL}}{G} \leq 2.4V$

Figure 3.28

A high gain (G = 100) single supply two op amp in-amp configuration is shown in Figure 3.29. Using the same equations, note that the voltage at V_1 can now swing between 0.124V and 4.876V. Again, V_{REF} is connected to 2.5V to allow for bipolar differential input and output signals.

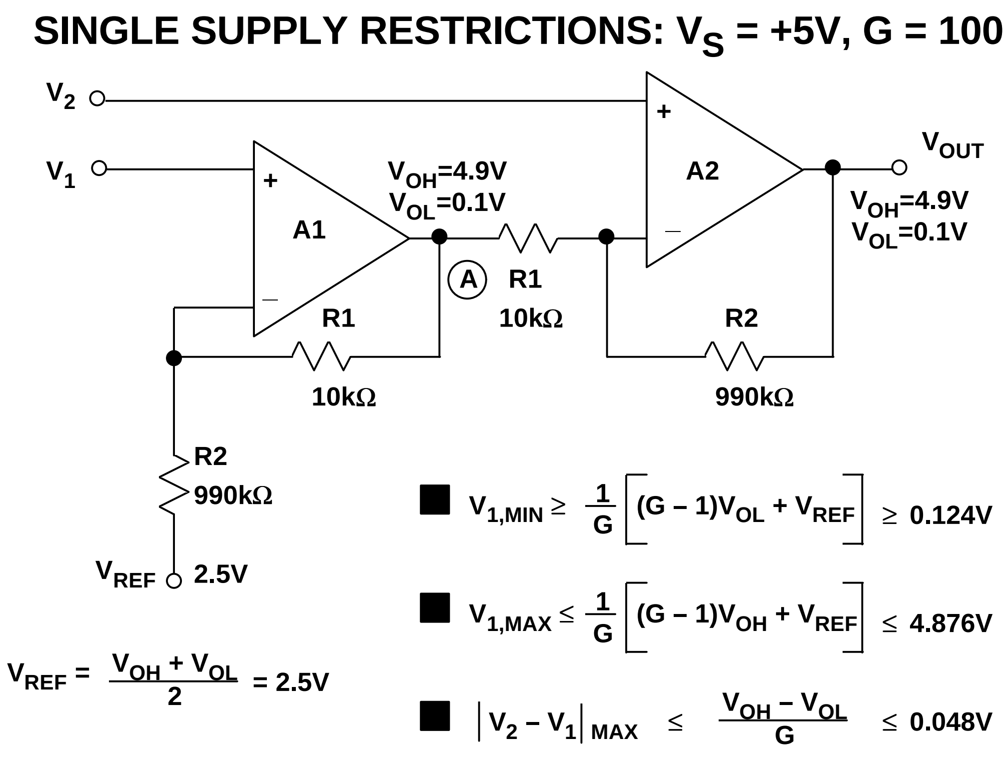


Figure 3.29

The above discussion shows that regardless of gain, the basic two op amp in-amp does not allow for zero-volt common mode input voltages when operated on a single supply. This limitation can be overcome using the circuit shown in Figure 3.30 which is implemented in the AD627 in-amp. Each op amp is composed of a PNP common emitter input stage and a gain stage, designated Q1/A1 and Q2/A2, respectively. The PNP transistors not only provide gain but also level shift the input signal positive by about 0.5V, thereby allowing the common mode input voltage to go to 0.1V below the negative supply rail. The maximum positive input voltage allowed is 1V less than the positive supply rail.

The AD627 in-amp delivers rail-to-rail output swing and operates over a wide supply voltage range (+2.7V to ±18V). Without R_G, the external gain setting resistor, the in-amp gain is 5. Gains up to 1000 can be set with a single external resistor. Common mode rejection of the AD627B at 60Hz with a 1kΩ source imbalance is 85dB when operating on a single +3V supply and G = 5. Even though the AD627 is a two op amp in-amp, a patented circuit keeps the CMR flat out to a much higher frequency than would be achievable with a conventional discrete two op amp in-amp. The AD627 data sheet (available at http://www.analog.com) has a detailed discussion of allowable input/output voltage ranges as a function of gain and power supply voltages. Key specifications for the AD627 are summarized in Figure 3.31.

AD627 IN-AMP ARCHITECTURE

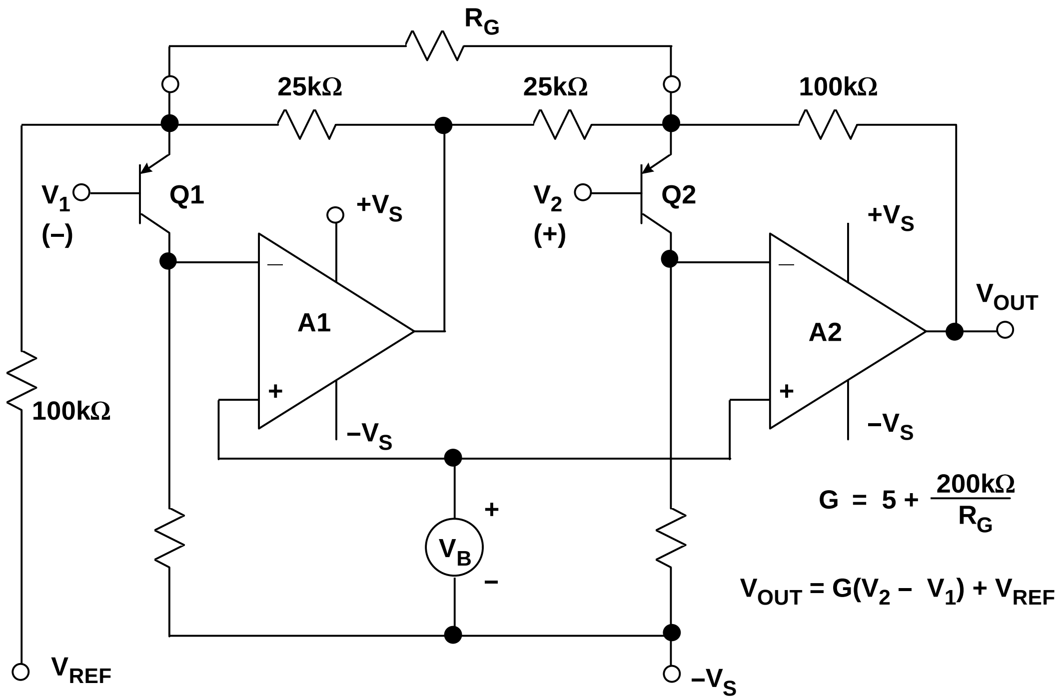


Figure 3.30

AD627 IN-AMP KEY SPECIFICATIONS

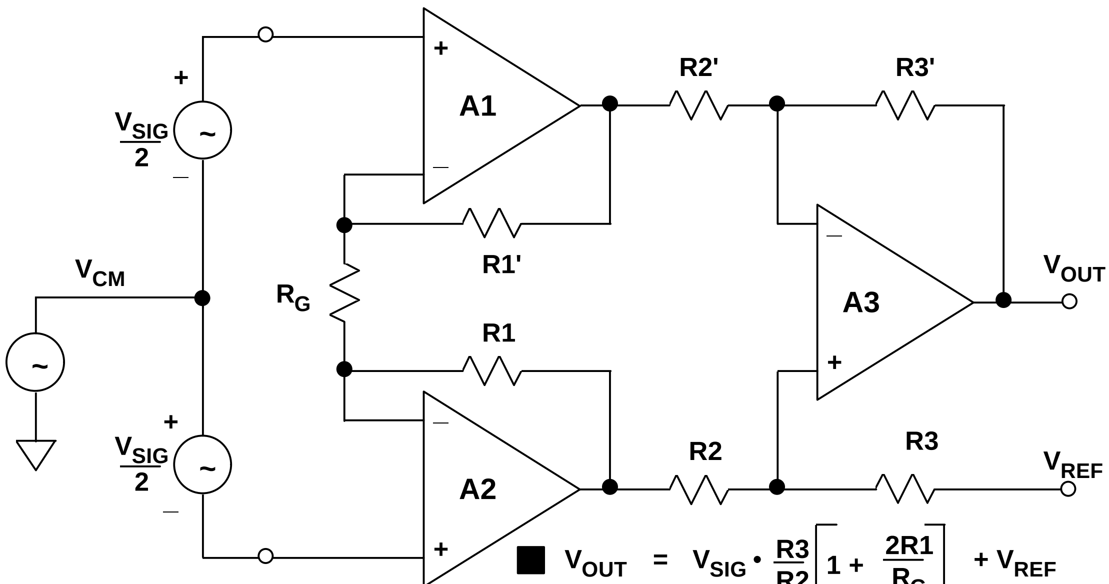
- **Wide Supply Range : +2.7V to ±18V**
- **Input Voltage Range: $-V_S - 0.1V$ to $+V_S - 1V$**
- **85µA Supply Current**
- **Gain Range: 5 to 1000**
- **75µV Maximum Input Offset Volage (AD627B)**
- **10ppm/°C Maximum Offset Voltage TC (AD627B)**
- **10ppm Gain Nonlinearity**
- **85dB CMR @ 60Hz, 1kΩ Source Imbalance (G = 5)**
- **3µV p-p 0.1Hz to 10Hz Input Voltage Noise (G = 5)**

Figure 3.31

For true balanced high impedance inputs, three op amps may be connected to form the in-amp shown in Figure 3.32. This circuit is typically referred to as the *three op amp in-amp*. The gain of the amplifier is set by the resistor, R_G, which may be internal, external, or (software or pin-strap) programmable. In this configuration, CMR depends upon the ratio matching of R3/R2 to R3'/R2'. Furthermore, common mode signals are only amplified by a factor of 1 regardless of gain (no common mode voltage will appear across R_G, hence, no common mode current will flow in it

because the input terminals of an op amp will have no significant potential difference between them). Thus, CMR will theoretically increase in direct proportion to gain. Large common mode signals (within the A1-A2 op amp headroom limits) may be handled at all gains. Finally, because of the symmetry of this configuration, common mode errors in the input amplifiers, if they track, tend to be canceled out by the subtractor output stage. These features explain the popularity of the three op amp in-amp configuration.

THREE OP AMP INSTRUMENTATION AMPLIFIER



- $V_{OUT} = V_{SIG} \bullet \frac{R3}{R2}\left[1 + \frac{2R1}{R_G}\right] + V_{REF}$
- $CMR \leq 20\log\left[\frac{GAIN \times 100}{\%\ MISMATCH}\right]$
- IF R2 = R3, $G = 1 + \frac{2R1}{R_G}$

Figure 3.32

The classic three op amp configuration has been used in a number of monolithic IC instrumentation amplifiers. Besides offering excellent matching between the three internal op amps, thin film laser trimmed resistors provide excellent ratio matching and gain accuracy at much lower cost than using discrete op amps and resistor networks. The AD620 is an excellent example of monolithic in-amp technology, and a simplified schematic is shown in Figure 3.33.

The AD620 is a highly popular in-amp and is specified for power supply voltages from ±2.3V to ±18V. Input voltage noise is only 9nV/√Hz @ 1kHz. Maximum input bias current is only 1nA maximum because of the Superbeta input stage.

Overvoltage protection is provided by the internal 400Ω thin-film current-limit resistors in conjunction with the diodes which are connected from the emitter-to-base of Q1 and Q2. The gain is set with a single external R_G resistor. The appropriate internal resistors are trimmed so that standard 1% or 0.1% resistors can be used to set the AD620 gain to popular gain values.

AD620 IN-AMP SIMPLIFIED SCHEMATIC

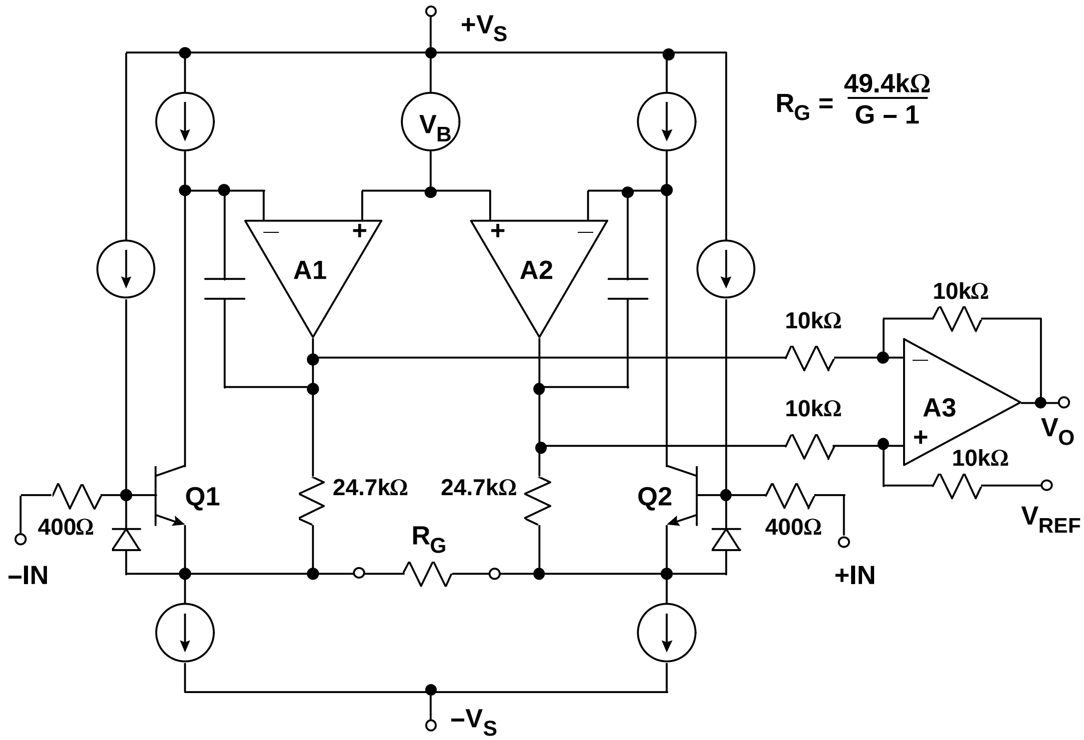


Figure 3.33

As in the case of the two op amp in-amp configuration, single supply operation of the three op amp in-amp requires an understanding of the internal node voltages. Figure 3.34 shows a generalized diagram of the in-amp operating on a single +5V supply. The maximum and minimum allowable output voltages of the individual op amps are designated V_{OH} (maximum high output) and V_{OL} (minimum low output) respectively. Note that the gain from the common mode voltage to the outputs of A1 and A2 is unity, and that *the sum of the common mode voltage and the signal voltage at these outputs must fall within the amplifier output voltage range*. It is obvious that this configuration cannot handle input common mode voltages of either zero volts or +5V because of saturation of A1 and A2. As in the case of the two op amp in-amp, the output reference is positioned halfway between V_{OH} and V_{OL} in order to allow for bipolar differential input signals.

This chapter has emphasized the operation of high performance linear circuits from a single, low-voltage supply (5V or less) is a common requirement. While there are many precision single supply operational amplifiers, such as the OP213, the OP291, and the OP284, and some good single-supply instrumentation amplifiers, the highest performance instrumentation amplifiers are still specified for dual-supply operation.

THREE OP AMP IN-AMP SINGLE +5V SUPPLY RESTRICTIONS

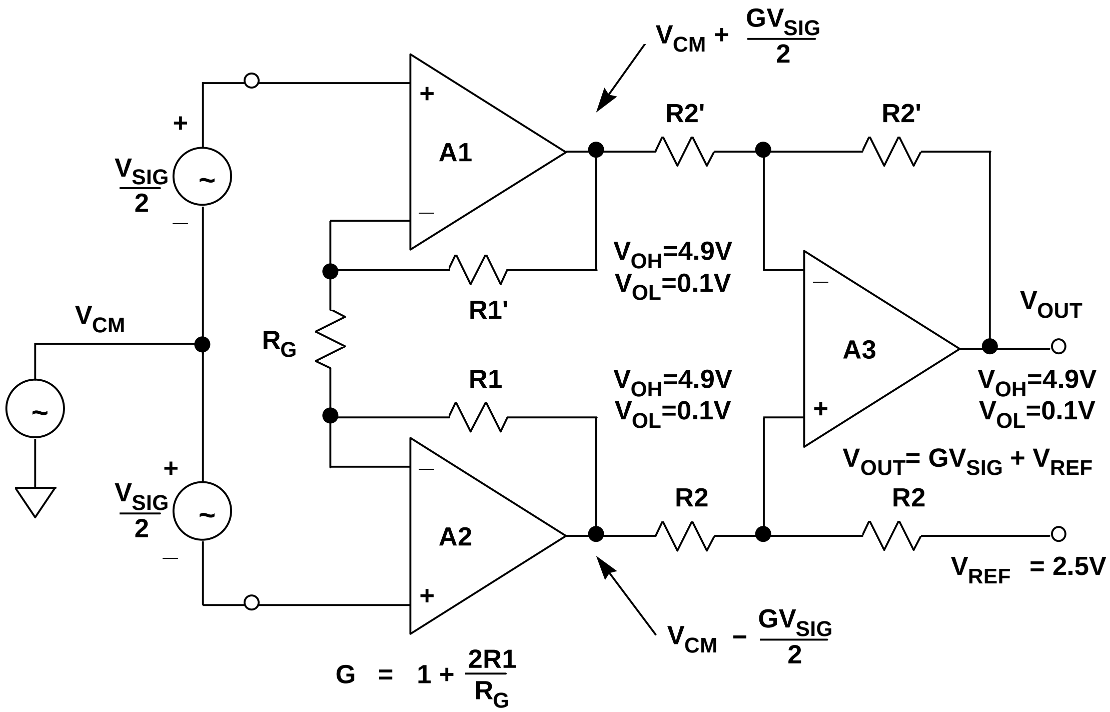


Figure 3.34

One way to achieve both high precision and single-supply operation takes advantage of the fact that several popular sensors (e.g. strain gauges) provide an output signal centered around the (approximate) mid-point of the supply voltage (or the reference voltage), where the inputs of the signal conditioning amplifier need not operate near "ground" or the positive supply voltage.

Under these conditions, a dual-supply instrumentation amplifier referenced to the supply mid-point followed by a "rail-to-rail" operational amplifier gain stage provides very high DC precision. Figure 3.35 illustrates one such high-performance instrumentation amplifier operating on a single, +5V supply. This circuit uses an AD620 low-cost precision instrumentation amplifier for the input stage, and an AD822 JFET-input dual rail-to-rail output operational amplifier for the output stage.

In this circuit, R3 and R4 form a voltage divider which splits the supply voltage in half to +2.5V, with fine adjustment provided by a trimming potentiometer, P1. This voltage is applied to the input of A1, an AD822 which buffers it and provides a low-impedance source needed to drive the AD620's reference pin. The AD620's Reference pin has a 10kΩ input resistance and an input signal current of up to 200μA. The other half of the AD822 is connected as a gain-of-3 inverter, so that it can output ±2.5V, "rail-to-rail," with only ±0.83V required of the AD620. This output voltage

level of the AD620 is well within the AD620's capability, thus ensuring high linearity for the "dual-supply" front end. *Note that the final output voltage must be measured with respect to the +2.5V reference, and not to GND.*

A PRECISION SINGLE-SUPPLY COMPOSITE IN-AMP WITH RAIL-TO-RAIL OUTPUT

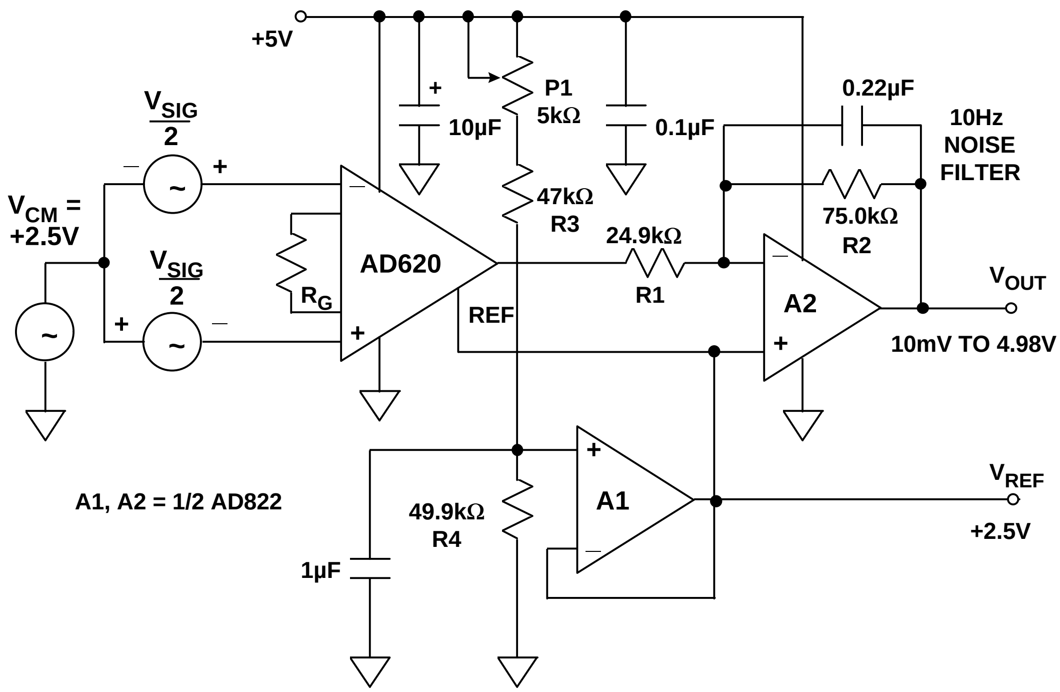


Figure 3.35

The general gain expression for this composite instrumentation amplifier is the product of the AD620 and the inverting amplifier gains:

$$\text{GAIN} = \left(\frac{49.4\,\text{k}\Omega}{R_G} + 1\right)\left(\frac{R2}{R1}\right).$$

For this example, an overall gain of 10 is realized with R_G = 21.5kΩ (closest standard value). The table (Figure 3.36) summarizes various R_G/gain values and performance.

In this application, the allowable input voltage on either input to the AD620 must lie between +2V and +3.5V in order to maintain linearity. For example, at an overall circuit gain of 10, the common mode input voltage range spans 2.25V to 3.25V, allowing room for the ±0.25V full-scale differential input voltage required to drive the output ±2.5V about V_{REF}.

The inverting configuration was chosen for the output buffer to facilitate system output offset voltage adjustment by summing currents into the A2 stage buffer's feedback summing node. These offset currents can be provided by an external DAC, or from a resistor connected to a reference voltage.

The AD822 rail-to-rail output stage exhibits a very clean transient response (not shown) and a small-signal bandwidth over 100kHz for gain configurations up to 300. Note that excellent linearity is maintained over 0.1V to 4.9V V_{OUT}. To reduce the effects of unwanted noise pickup, a capacitor is recommended across A2's feedback resistance to limit the circuit bandwidth to the frequencies of interest.

PERFORMANCE SUMMARY OF THE +5V SINGLE-SUPPLY AD620/AD822 COMPOSITE IN-AMP

CIRCUIT GAIN	R_G (Ω)	V_{OS}, RTI (µV)	TC V_{OS}, RTI (µV/°C)	NONLINEARITY (ppm) *	BANDWIDTH (kHz)**
10	21.5k	1000	1000	< 50	600
30	5.49k	430	430	< 50	600
100	1.53k	215	215	< 50	300
300	499	150	150	< 50	120
1000	149	150	150	< 50	30

* Nonlinearity Measured Over Output Range: 0.1V < V_{OUT} < 4.90V
** Without 10Hz Noise Filter

Figure 3.36

In cases where zero-volt inputs are required, the AD623 single supply in-amp configuration shown in Figure 3.37 offers an attractive solution. The PNP emitter follower level shifters, Q1/Q2, allow the input signal to go 150mV below the negative supply and to within 1.5V of the positive supply. The AD623 is fully specified for single power supplies between +3V and +12V and dual supplies between ±2.5V and ±6V (see Figure 3.38). The AD623 data sheet (available at http://www.analog.com) contains an excellent discussion of allowable input/output voltage ranges as a function of gain and power supply voltages.

AD623 SINGLE-SUPPLY IN-AMP ARCHITECTURE

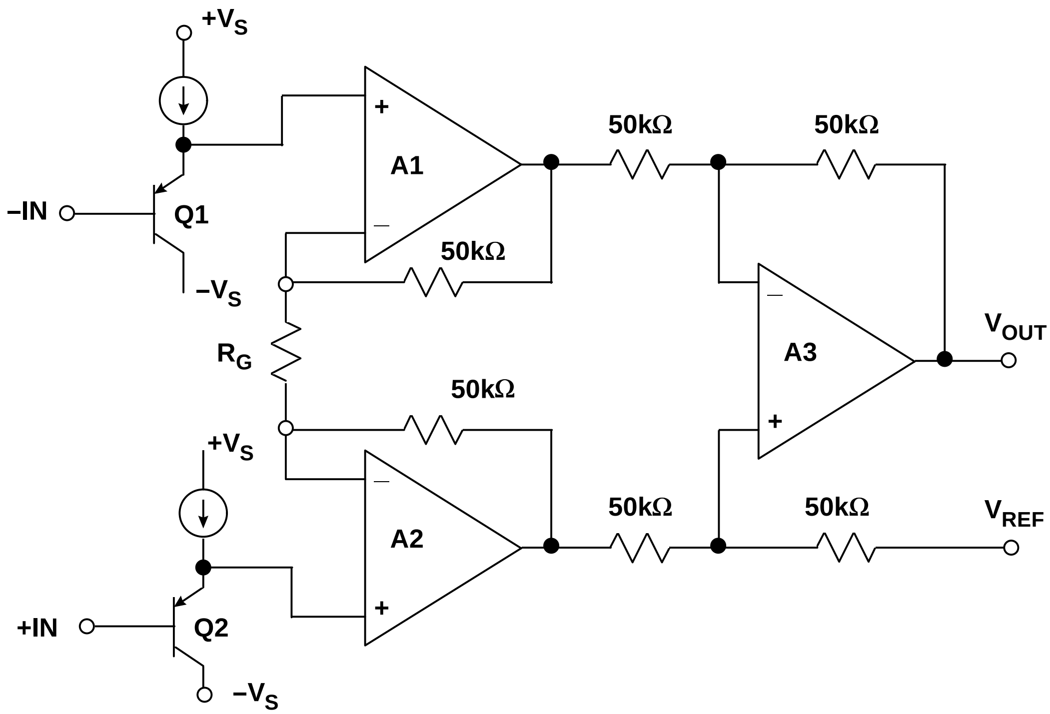


Figure 3.37

AD623 IN-AMP KEY SPECIFICATIONS

- Wide Supply Range: +3V to ±6V
- Input Voltage Range: $-V_S$ – 0.15V to $+V_S$ – 1.5V
- 575µA Maximum Supply Current
- Gain Range: 1 to 1000
- 100µV Maximum Input Offset Voltage (AD623B)
- 1µV/°C Maximum Offset Voltage TC (AD623B)
- 50ppm Gain Nonlinearity
- 105dB CMR @ 60Hz, 1kΩ Source Imbalance, G ≥ 100
- 3µV p-p 0.1Hz to 10Hz Input Voltage Noise (G = 1)

Figure 3.38

Instrumentation Amplifier DC Error Sources

The DC and noise specifications for instrumentation amplifiers differ slightly from conventional op amps, so some discussion is required in order to fully understand the error sources.

The gain of an in-amp is usually set by a single resistor. If the resistor is external to the in-amp, its value is either calculated from a formula or chosen from a table on the data sheet, depending on the desired gain.

Absolute value laser wafer trimming allows the user to program gain accurately with this single resistor. The absolute accuracy and temperature coefficient of this resistor directly affects the in-amp gain accuracy and drift. Since the external resistor will never exactly match the internal thin film resistor tempcos, a low TC (<25ppm/°C) metal film resistor should be chosen, preferably with a 0.1% or better accuracy.

Often specified as having a gain range of 1 to 1000, or 1 to 10,000, many in-amps will work at higher gains, but the manufacturer will not guarantee a specific level of performance at these high gains. In practice, as the gain-setting resistor becomes smaller, any errors due to the resistance of the metal runs and bond wires become significant. These errors, along with an increase in noise and drift, may make higher single-stage gains impractical. In addition, input offset voltages can become quite sizable when reflected to output at high gains. For instance, a 0.5mV input offset voltage becomes 5V at the output for a gain of 10,000. For high gains, the best practice is to use an instrumentation amplifier as a preamplifier then use a post amplifier for further amplification.

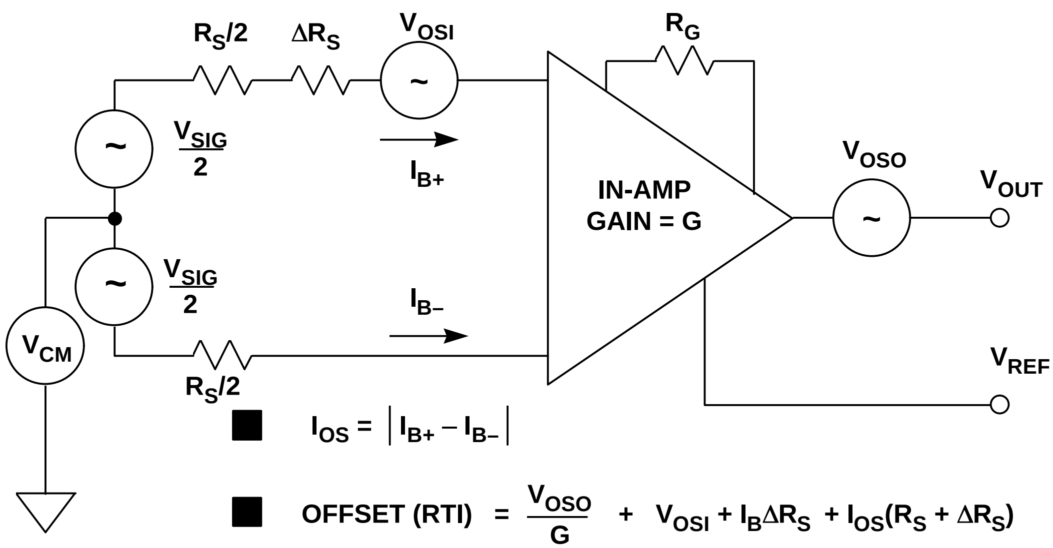
In a pin-programmable gain in-amp such as the AD621, the gain setting resistors are internal, well matched, and the gain accuracy and gain drift specifications include their effects. The AD621 is otherwise generally similar to the externally gain-programmed AD620.

The *gain error* specification is the maximum deviation from the gain equation. Monolithic in-amps such as the AD624C have very low factory trimmed gain errors, with its maximum error of 0.02% at G = 1 and 0.25% at G = 500 being typical for this high quality in-amp. Notice that the gain error increases with increasing gain. Although externally connected gain networks allow the user to set the gain exactly, the temperature coefficients of the external resistors and the temperature differences between individual resistors within the network all contribute to the overall gain error. If the data is eventually digitized and presented to a digital processor, it may be possible to correct for gain errors by measuring a known reference voltage and then multiplying by a constant.

Nonlinearity is defined as the maximum deviation from a straight line on the plot of output versus input. The straight line is drawn between the end-points of the actual transfer function. Gain nonlinearity in a high quality in-amp is usually 0.01% (100ppm) or less, and is relatively insensitive to gain over the recommended gain range.

The total input offset voltage of an in-amp consists of two components (see Figure 3.39). Input offset voltage, V_{OSI}, is that component of input offset which is reflected to the output of the in-amp by the gain G. Output offset voltage, V_{OSO}, is independent of gain. At low gains, output offset voltage is dominant, while at high gains input offset dominates. The output offset voltage drift is normally specified as drift at G=1 (where input effects are insignificant), while input offset voltage drift is given by a drift specification at a high gain (where output offset effects are negligible). The total output offset error, referred to the input (RTI), is equal to $V_{OSI} + V_{OSO}/G$. In-amp data sheets may specify V_{OSI} and V_{OSO} separately or give the total RTI input offset voltage for different values of gain.

IN-AMP OFFSET VOLTAGE MODEL



- $I_{OS} = \left| I_{B+} - I_{B-} \right|$
- $\text{OFFSET (RTI)} = \dfrac{V_{OSO}}{G} + V_{OSI} + I_B \Delta R_S + I_{OS}(R_S + \Delta R_S)$
- $\text{OFFSET (RTO)} = V_{OSO} + G\left[V_{OSI} + I_B \Delta R_S + I_{OS}(R_S + \Delta R_S)\right]$

Figure 3.39

Input bias currents may also produce offset errors in in-amp circuits (see Figure 3.39). If the source resistance, R_S, is unbalanced by an amount, ΔR_S, (often the case in bridge circuits), then there is an additional input offset voltage error due to the bias current, equal to $I_B \Delta R_S$ (assuming that $I_{B+} \approx I_{B-} = I_B$). This error is reflected to the output, scaled by the gain G. The input offset current, I_{OS}, creates an input offset voltage error across the source resistance, $R_S + \Delta R_S$, equal to $I_{OS}(R_S + \Delta R_S)$, which is also reflected to the output by the gain, G.

In-amp common mode error is a function of both gain and frequency. Analog Devices specifies in-amp CMR for a 1kΩ source impedance unbalance at a frequency of 60Hz. The RTI common mode error is obtained by dividing the common mode voltage, V_{CM}, by the common mode rejection ratio, CMRR.

Power supply rejection (PSR) is also a function of gain and frequency. For in-amps, it is customary to specify the sensitivity to each power supply separately. Now that all DC error sources have been accounted for, a worst case DC error budget can be calculated by reflecting all the sources to the in-amp input (Figure 3.40).

INSTRUMENTATION AMPLIFIER AMPLIFIER DC ERRORS REFERRED TO THE INPUT (RTI)

ERROR SOURCE	RTI VALUE
Gain Accuracy (ppm)	Gain Accuracy × FS Input
Gain Nonlinearity (ppm)	Gain Nonlinearity × FS Input
Input Offset Voltage, V_{OSI}	V_{OSI}
Output Offset Voltage, V_{OSO}	$V_{OSO} \div G$
Input Bias Current, I_B, Flowing in ΔR_S	$I_B \Delta R_S$
Input Offset Current, I_{OS}, Flowing in R_S	$I_{OS}(R_S + \Delta R_S)$
Common Mode Input Voltage, V_{CM}	$V_{CM} \div CMRR$
Power Supply Variation, ΔV_S	$\Delta V_S \div PSRR$

Figure 3.40

Instrumentation Amplifier Noise Sources

Since in-amps are primarily used to amplify small precision signals, it is important to understand the effects of all the associated noise sources. The in-amp noise model is shown in Figure 3.41. There are two sources of input voltage noise. The first is represented as a noise source, V_{NI}, in series with the input, as in a conventional op amp circuit. This noise is reflected to the output by the in-amp gain, G. The second noise source is the output noise, V_{NO}, represented as a noise voltage in series with the in-amp output. The output noise, shown here referred to V_{OUT}, can be referred to the input by dividing by the gain, G.

There are two noise sources associated with the input noise currents I_{N+} and I_{N-}. Even though I_{N+} and I_{N-} are usually equal ($I_{N+} \approx I_{N-} = I_N$), they are uncorrelated, and therefore, the noise they each create must be summed in a root-sum-squares (RSS) fashion. I_{N+} flows through one half of R_S, and I_{N-} the other half. This generates two noise voltages, each having an amplitude, $I_N R_S/2$. Each of these two noise sources is reflected to the output by the in-amp gain, G.

The total output noise is calculated by combining all four noise sources in an RSS manner:

$$\text{NOISE (RTO)} = \sqrt{BW}\sqrt{{V_{NO}}^2 + G^2\left({V_{NI}}^2 + \frac{{I_{N+}}^2{R_S}^2}{4} + \frac{{I_{N-}}^2{R_S}^2}{4}\right)}\ .$$

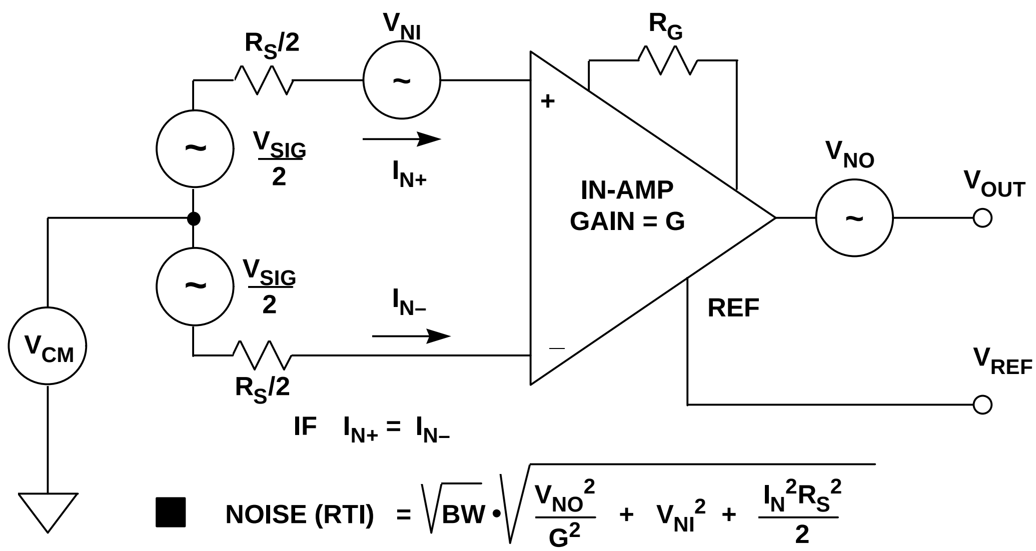
If $I_{N+} = I_{N-} = I_N$,

$$\text{NOISE (RTO)} = \sqrt{BW}\sqrt{V_{NO}^2 + G^2\left(V_{NI}^2 + \frac{I_N^2 R_S^2}{2}\right)}.$$

The total noise, referred to the input (RTI) is simply the above expression divided by the in-amp gain, G:

$$\text{NOISE (RTI)} = \sqrt{BW}\sqrt{\frac{V_{NO}^2}{G^2} + \left(V_{NI}^2 + \frac{I_N^2 R_S^2}{2}\right)}.$$

IN-AMP NOISE MODEL



- $\text{NOISE (RTI)} = \sqrt{BW} \bullet \sqrt{\frac{V_{NO}^2}{G^2} + V_{NI}^2 + \frac{I_N^2 R_S^2}{2}}$
- $\text{NOISE (RTO)} = \sqrt{BW} \bullet \sqrt{V_{NO}^2 + G^2\left[V_{NI}^2 + \frac{I_N^2 R_S^2}{2}\right]}$
- BW = 1.57 × IN-AMP Bandwidth @ Gain = G

Figure 3.41

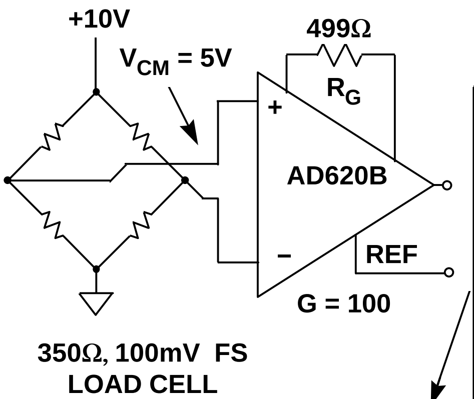
In-amp data sheets often present the total voltage noise RTI as a function of gain. This noise spectral density includes both the input (V_{NI}) and output (V_{NO}) noise contributions. The input current noise spectral density is specified separately. As in the case of op amps, the total noise RTI must be integrated over the in-amp closed-loop bandwidth to compute the RMS value. The bandwidth may be determined from data sheet curves which show frequency response as a function of gain.

In-Amp Bridge Amplifier Error Budget Analysis

It is important to understand in-amp error sources in a typical application. Figure 3.42 shows a 350Ω load cell which has a fullscale output of 100mV when excited with a 10V source. The AD620 is configured for a gain of 100 using the external 499Ω gain-setting resistor. The table shows how each error source contributes to the

total unadjusted error of 2145ppm. The gain, offset, and CMR errors can be removed with a system calibration. The remaining errors - gain nonlinearity and 0.1Hz to 10Hz noise - cannot be removed with calibration and limit the system resolution to 42.8ppm (approximately 14-bit accuracy).

AD620B BRIDGE AMPLIFIER DC ERROR BUDGET



AD620B SPECS @ +25°C, ±15V
$V_{OSI} + V_{OSO}/G$ = 55µV max
I_{OS} = 0.5nA max
Gain Error = 0.15%
Gain Nonlinearity = 40ppm
0.1Hz to 10Hz Noise = 280nVp-p
CMR = 120dB @ 60Hz

MAXIMUM ERROR CONTRIBUTION, +25°C
FULLSCALE: V_{IN} = 100mV, V_{OUT} = 10V

V_{OS}	55µV ÷ 100mV	550ppm
I_{OS}	350Ω × 0.5nA ÷ 100mV	1.8ppm
Gain Error	0.15%	1500ppm
Gain Nonlinearity	40ppm	40ppm
CMR Error	120dB 1ppm × 5V ÷ 100mV	50ppm
0.1Hz to 10Hz 1/f Noise	280nV ÷ 100mV	2.8ppm
Total Unadjusted Error	≈ 9 Bits Accurate	2145ppm
Resolution Error	≈ 14 Bits Accurate	42.8ppm

Figure 3.42

In-Amp Performance Tables

Figure 3.43 shows a selection of precision in-amps designed primarily for operation on dual supplies. It should be noted that the AD620 is capable of single +5V supply operation (see Figure 3.35), but neither its input nor its output are capable of rail-to-rail swings.

Instrumentation amplifiers specifically designed for single supply operation are shown in Figure 3.44. It should be noted that although the specifications in the figure are given for a single +5V supply, all of the amplifiers are also capable of dual supply operation and are specified for both dual and single supply operation on their data sheets. In addition, the AD623 and AD627 will operate on a single +3V supply.

The AD626 is not a true in-amp but is a differential amplifier with a thin-film input attenuator which allows the common mode voltage to exceed the supply voltages. This device is designed primarily for high and low-side current-sensing applications. It will also operate on a single +3V supply.

PRECISION IN-AMPS:
DATA FOR V_S = ±15V, G = 1000

	Gain Accuracy *	Gain Nonlinearity	V_{OS} Max	V_{OS} TC	CMR Min	0.1Hz to 10Hz p-p Noise
AD524C	0.5% / P	100ppm	50µV	0.5µV/°C	120dB	0.3µV
AD620B	0.5% / R	40ppm	50µV	0.6µV/°C	120dB	0.28µV
AD621B[1]	0.05% / P	10ppm	50µV	1.6µV/°C	100dB	0.28µV
AD622	0.5% / R	40ppm	125µV	1µV/°C	103dB	0.3µV
AD624C[2]	0.25% / R	50ppm	25µV	0.25µV/°C	130dB	0.2µV
AD625C	0.02% / R	50ppm	25µV	0.25µV/°C	125dB	0.2µV
AMP01A	0.6% / R	50ppm	50µV	0.3µV/°C	125dB	0.12µV
AMP02E	0.5% / R	60ppm	100µV	2µV/°C	115dB	0.4µV

* / P = Pin Programmable
* / R = Resistor Programmable

[1] G = 100
[2] G = 500

Figure 3.43

SINGLE SUPPLY IN-AMPS:
DATA FOR V_S = +5V, G = 1000

	Gain Accuracy *	Gain Nonlinearity	V_{OS} Max	V_{OS} TC	CMR Min	0.1Hz to 10Hz p-p Noise	Supply Current
AD623B	0.5% / R	50ppm	100µV	1µV/°C	105dB	1.5µV	575µA
AD627B	0.35% / R	10ppm	75µV	1µV/°C	85dB	1.5µV	85µA
AMP04E	0.4% / R	250ppm	150µV	3µV/°C	90dB	0.7µV	290µA
AD626B[1]	0.6% / P	200ppm	2.5mV	6µV/°C	80dB	2µV	700µA

* / P = Pin Programmable
* / R = Resistor Programmable

[1] Differential Amplifier, G = 100

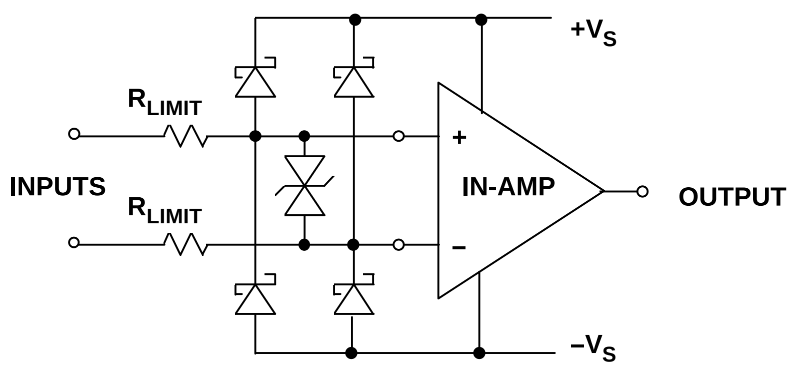
Figure 3.44

In-Amp Input Overvoltage Protection

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. The manufacturer's "absolute maximum" input ratings for the device should be closely observed. As with op amps, many in-amps have absolute maximum input voltage specifications equal to $\pm V_S$. External series resistors (for current limiting) and Schottky diode clamps may be used to prevent overload, if necessary. Some instrumentation amplifiers have built-in overload protection circuits in the form of series resistors (thin film) or series-protection FETs. In-amps such as the AMP-02 and the AD524 utilize series-protection FETs, because they act as a low impedance during normal operation, and a high impedance during fault conditions.

An additional Transient Voltage Suppresser (TVS) may be required across the input pins to limit the maximum differential input voltage. This is especially applicable to three op amp in-amps operating at high gain with low values of R_G. A more detailed discussion of input voltage and EMI/RFI protection can be found in Section 10 of this book.

INSTRUMENTATION AMPLIFIER INPUT OVERVOLTAGE CONSIDERATIONS



- **Always Observe Absolute Maximum Data Sheet Specs!**
- **Schottky Diode Clamps to the Supply Rails Will Limit Input to Approximately $\pm V_S$ ±0.3V, TVSs Limit Differential Voltage**
- **External Resistors (or Internal Thin-Film Resistors) Can Limit Input Current, but will Increase Noise**
- **Some In-Amps Have Series-Protection Input FETs for Lower Noise and Higher Input Over-Voltages (up to ±60V, Depending on Device)**

Figure 3.45

CHOPPER STABILIZED AMPLIFIERS

For the lowest offset and drift performance, chopper-stabilized amplifiers may be the only solution. The best bipolar amplifiers offer offset voltages of 10µV and 0.1µV/ºC drift. Offset voltages less than 5µV with practically no measurable offset drift are obtainable with choppers, albeit with some penalties.

The basic chopper amplifier circuit is shown in Figure 3.46. When the switches are in the "Z" (auto-zero) position, capacitors C2 and C3 are charged to the amplifier input and output offset voltage, respectively. When the switches are in the "S" (sample) position, V_{IN} is connected to V_{OUT} through the path comprised of R1, R2, C2, the amplifier, C3, and R3. The chopping frequency is usually between a few hundred Hz and several kHz, and it should be noted that because this is a sampling system, the input frequency must be much less than one-half the chopping frequency in order to prevent errors due to aliasing. The R1/C1 combination serves as an antialiasing filter. It is also assumed that after a steady state condition is reached, there is only a minimal amount of charge transferred during the switching cycles. The output capacitor, C4, and the load, R_L, must be chosen such that there is minimal V_{OUT} droop during the auto-zero cycle.

CLASSIC CHOPPER AMPLIFIER

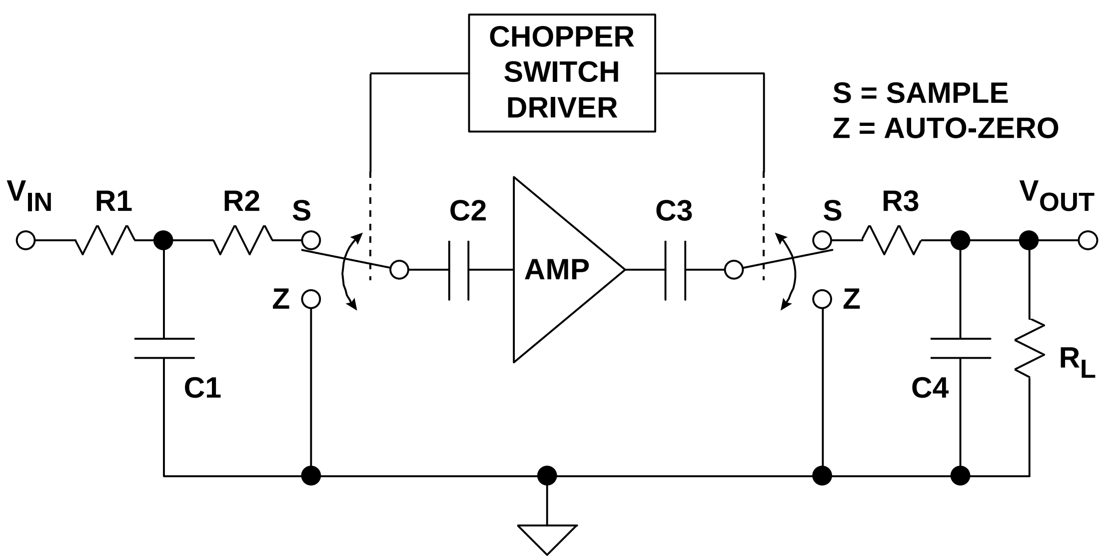


Figure 3.46

The basic chopper amplifier of Figure 3.46 can pass only very low frequencies because of the input filtering required to prevent aliasing. The *chopper-stabilized* architecture shown in Figure 3.47 is most often used in chopper amplifier implementations. In this circuit, A1 is the *main* amplifier, and A2 is the *nulling* amplifier. In the sample mode (switches in "S" position), the nulling amplifier, A2, monitors the input offset voltage of A1 and drives its output to zero by applying a suitable correcting voltage at A1's null pin. Note, however, that A2 also has an input offset voltage, so it must correct its own error before attempting to null A1's offset. This is achieved in the auto-zero mode (switches in "Z" position) by momentarily disconnecting A2 from A1, shorting its inputs together, and coupling its output to its own null pin. During the auto-zero mode, the correction voltage for A1 is momentarily held by C1. Similarly, C2 holds the correction voltage for A2 during the sample mode. In modern IC chopper-stabilized op amps, the storage capacitors C1 and C2 are on-chip.

CHOPPER STABILIZED AMPLIFIER

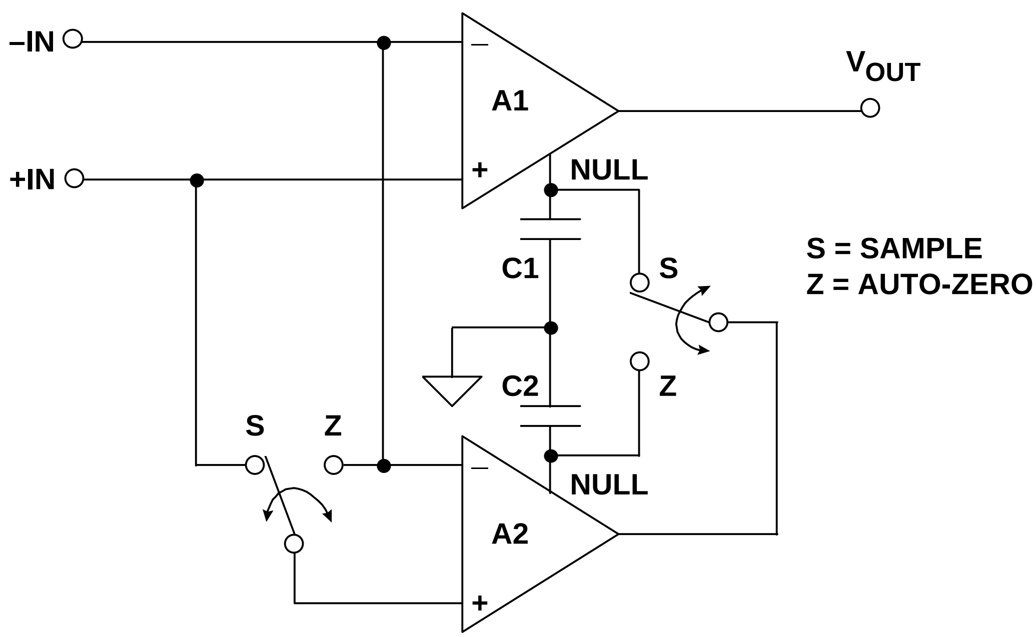


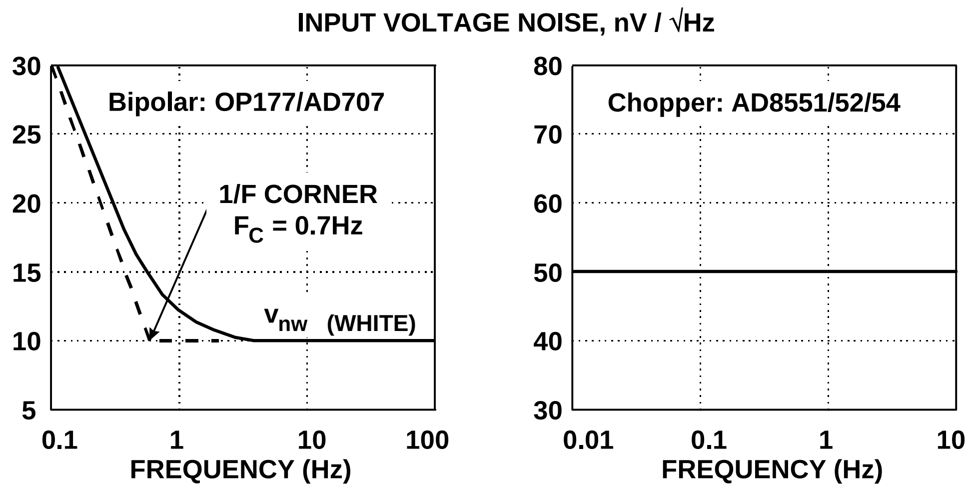
Figure 3.47

Note in this architecture that the input signal is always connected to the output through A1. The bandwidth of A1 thus determines the overall signal bandwidth, and the input signal is not limited to less than one-half the chopping frequency as in the case of the traditional chopper amplifier architecture. However, the switching action does produce small transients at the chopping frequency which can mix with the input signal frequency and produce in-band distortion.

It is interesting to consider the effects of a chopper amplifier on low frequency 1/f noise. If the chopping frequency is considerably higher than the 1/f corner frequency of the input noise, the chopper-stabilized amplifier continuously nulls out the 1/f noise on a sample-by-sample basis. Theoretically, a chopper op amp therefore has no 1/f noise. However, the chopping action produces wideband noise which is generally much worse than that of a precision bipolar op amp.

Figure 3.48 shows the noise of a precision bipolar amplifier (OP177/AD707) versus that of the AD8551/52/54 chopper-stabilized op amp. The peak-to-peak noise in various bandwidths is calculated for each in the table below the graphs. Note that as the frequency is lowered, the chopper amplifier noise continues to drop, while the bipolar amplifier noise approaches a limit determined by the 1/f corner frequency and its white noise (see Figure 3.9). At a very low frequency, the noise performance of the chopper is superior to that of the bipolar op amp.

NOISE: BIPOLAR VS. CHOPPER AMPLIFIER



NOISE BW	BIPOLAR (OP177/AD707)	CHOPPER (AD8551/52/54)
0.1Hz to 10Hz	0.238µV p-p	1.04 µV p-p
0.01Hz to 1Hz	0.135µV p-p	0.33µV p-p
0.001Hz to 0.1Hz	0.120µV p-p	0.104µV p-p
0.0001Hz to 0.01Hz	0.118µV p-p	0.033µV p-p

Figure 3.48

The AD8551/8552/8554 family of chopper-stabilized op amps offers rail-to-rail input and output single supply operation, low offset voltage, and low offset drift. The storage capacitors are internal to the IC, and no external capacitors other than standard decoupling capacitors are required. Key specifications for the devices are given in Figure 3.49. It should be noted that extreme care must be taken when applying these devices to avoid parasitic thermocouple effects in order to fully realize the offset and drift performance. A further discussion of parasitic thermocouples can be found in Section 10.

AD8551/52/54 CHOPPER STABILIZED RAIL-TO-RAIL INPUT/OUTPUT AMPLIFIERS

- **Single Supply: +3V to +5V**
- **5µV Max. Input Offset Voltage**
- **0.04µV/°C Input Offset Voltage Drift**
- **120dB CMR, PSR**
- **800µA Supply Current / Op Amp**
- **100µs Overload Recovery Time**
- **50nV/√Hz Input Voltage Noise**
- **1.5MHz Gain-Bandwidth Product**
- **Single (AD8551), Dual (AD8552) and Quad (AD8554)**

Figure 3.49

ISOLATION AMPLIFIERS

There are many applications where it is desirable, or even essential, for a sensor to have no direct ("galvanic") electrical connection with the system to which it is supplying data, either in order to avoid the possibility of dangerous voltages or currents from one half of the system doing damage in the other, or to break an intractable ground loop. Such a system is said to be "isolated", and the arrangement which passes a signal without galvanic connections is known as an "isolation barrier".

The protection of an isolation barrier works in both directions, and may be needed in either, or even in both. The obvious application is where a sensor may accidentally encounter high voltages, and the system it is driving must be protected. Or a sensor may need to be isolated from accidental high voltages arising downstream, in order to protect its environment: examples include the need to prevent the ignition of explosive gases by sparks at sensors and the protection from electric shock of patients whose ECG, EEG or EMG is being monitored. The ECG case is interesting, as protection may be required in *both* directions: the patient must be protected from accidental electric shock, but if the patient's heart should stop, the ECG machine must be protected from the very high voltages (>7.5 kV) applied to the patient by the defibrillator which will be used to attempt to restart it.

APPLICATIONS FOR ISOLATION AMPLIFIERS

- **Sensor is at a High Potential Relative to Other Circuitry (or may become so under Fault Conditions)**
- **Sensor May Not Carry Dangerous Voltages, Irrespective of Faults in Other Circuitry (e.g. Patient Monitoring and Intrinsically Safe Equipment for use with Explosive Gases)**
- **To Break Ground Loops**

Figure 3.50

Just as interference, or *unwanted* information, may be coupled by electric or magnetic fields, or by electromagnetic radiation, these phenomena may be used for the transmission of *wanted* information in the design of isolated systems. The most common isolation amplifiers use transformers, which exploit magnetic fields, and another common type uses small high voltage capacitors, exploiting electric fields. Opto-isolators, which consist of an LED and a photocell, provide isolation by using light, a form of electromagnetic radiation. Different isolators have differing performance: some are sufficiently linear to pass high accuracy analog signals across an isolation barrier, with others the signal may need to be converted to digital form before transmission, if accuracy is to be maintained, a common application for V/F converters.

Transformers are capable of analog accuracy of 12-16 bits and bandwidths up to several hundred kHz, but their maximum voltage rating rarely exceeds 10kV, and is often much lower. Capacitively coupled isolation amplifiers have lower accuracy, perhaps 12-bits maximum, lower bandwidth, and lower voltage ratings - but they are cheap. Optical isolators are fast and cheap, and can be made with very high voltage ratings (4 -7kV is one of the more common ratings), but they have poor analog domain linearity, and are not usually suitable for direct coupling of precision analog signals.

Linearity and isolation voltage are not the only issues to be considered in the choice of isolation systems. Power is essential. Both the input and the output circuitry must be powered, and unless there is a battery on the isolated side of the isolation barrier (which is possible, but rarely convenient), some form of isolated power must be provided. Systems using transformer isolation can easily use a transformer (either the signal transformer or another one) to provide isolated power, but it is impractical to transmit useful amounts of power by capacitive or optical means. Systems using these forms of isolation must make other arrangements to obtain isolated power supplies - this is a powerful consideration in favor of choosing transformer isolated isolation amplifiers: they almost invariably include an isolated power supply.

The isolation amplifier has an input circuit that is galvanically isolated from the power supply and the output circuit. In addition, there is minimal capacitance

between the input and the rest of the device. Therefore, there is no possibility for DC current flow, and minimum AC coupling. Isolation amplifiers are intended for applications requiring safe, accurate measurement of low frequency voltage or current (up to about 100kHz) in the presence of high common-mode voltage (to thousands of volts) with high common mode rejection. They are also useful for line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements, where DC and line-frequency leakage must be maintained at levels well below certain mandated minimums. Principal applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment, and industrial process control systems.

In the basic two-port form, the output and power circuits are not isolated from one another. In the three-port isolator shown in Figure 3.51, the input circuits, output circuits, and power source are all isolated from one another. The figure shows the circuit architecture of a self-contained isolator, the AD210. An isolator of this type requires power from a two-terminal DC power supply. An internal oscillator (50kHz) converts the DC power to AC, which is transformer-coupled to the shielded input section, then converted to DC for the input stage and the auxiliary power output. The AC carrier is also modulated by the amplifier output, transformer-coupled to the output stage, demodulated by a phase-sensitive demodulator (using the carrier as the reference), filtered, and buffered using isolated DC power derived from the carrier. The AD210 allows the user to select gains from 1 to 100 using an external resistor. Bandwidth is 20kHz, and voltage isolation is 2500V RMS (continuous) and ± 3500V peak (continuous).

AD210 3-PORT ISOLATION AMPLIFIER

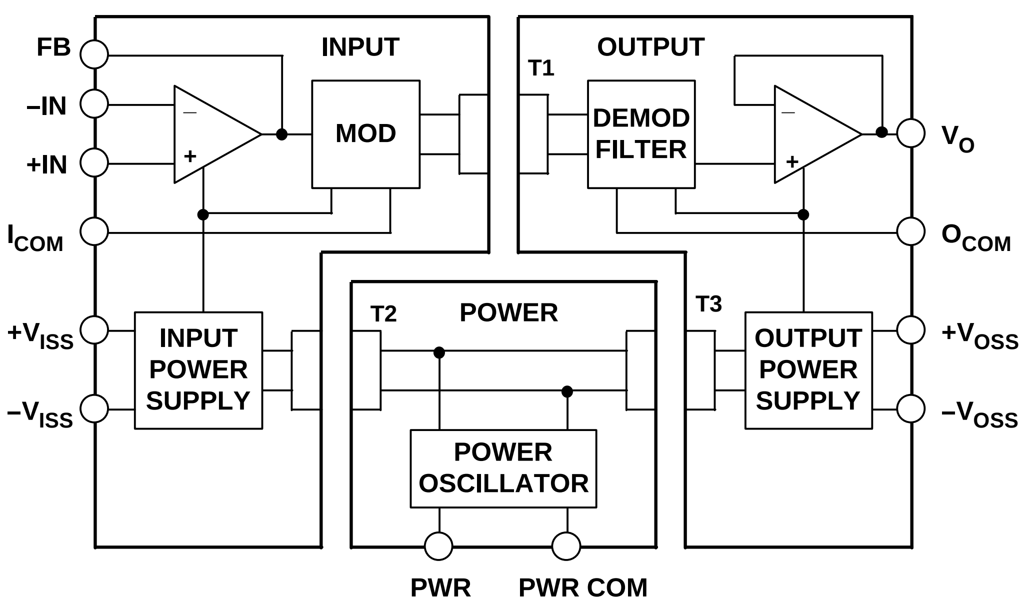


Figure 3.51

The AD210 is a 3-port isolation amplifier: the power circuitry is isolated from both the input and the output stages and may therefore be connected to either - or to neither. It uses transformer isolation to achieve 3500V isolation with 12-bit accuracy. Key specifications for the AD210 are summarized in Figure 3.52.

AD210 ISOLATION AMPLIFIER KEY FEATURES

- **Transformer Coupled**
- **High Common Mode Voltage Isolation:**
  - **2500V RMS Continuous**
  - **±3500V Peak Continuous**
- **Wide Bandwidth: 20kHz (Full Power)**
- **0.012% Maximum Linearity Error**
- **Input Amplifier: Gain 1 to 100**
- **Isolated Input and Output Power Supplies, ±15V, ±5mA**

Figure 3.52

A typical isolation amplifier application using the AD210 is shown in Figure 3.53. The AD210 is used with an AD620 instrumentation amplifier in a current-sensing system for motor control. The input of the AD210, being isolated, can be connected to a 110 or 230 V power line without any protection, and the isolated ±15 V powers the AD620, which senses the voltage drop in a small current sensing resistor. The 110 or 230V RMS common-mode voltage is ignored by the isolated system. The AD620 is used to improve system accuracy: the V_{OS} of the AD210 is 15mV, while the AD620 has V_{OS} of 30µV and correspondingly lower drift. If higher DC offset and drift are acceptable, the AD620 may be omitted, and the AD210 used directly at a closed loop gain of 100.

MOTOR CONTROL CURRENT SENSING

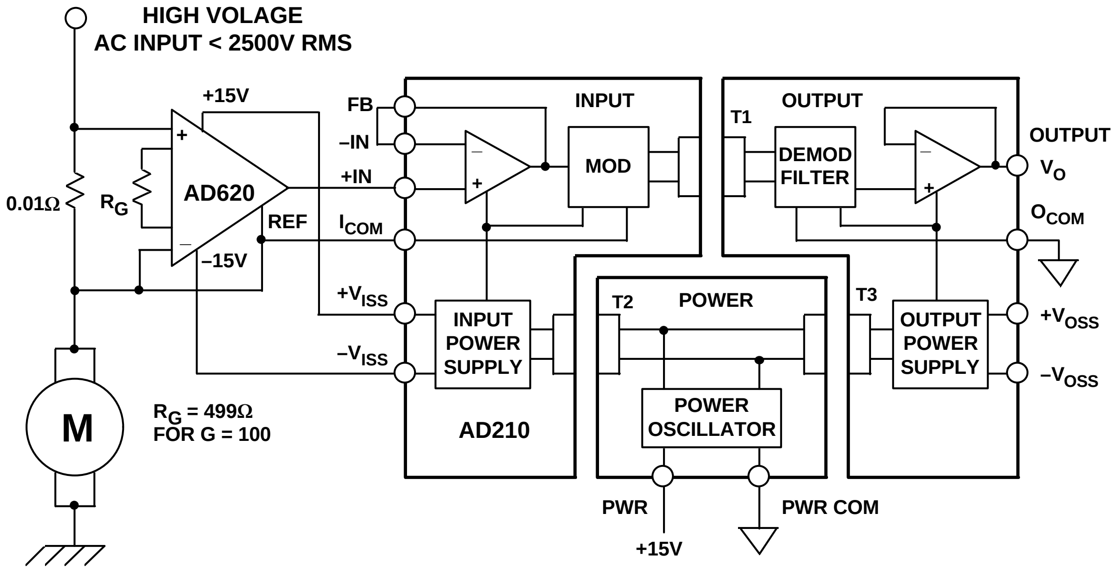


Figure 3.53

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